Sherief M. Reda – Curriculum Vitae

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Legal Name: Sherief M. Reda El-Edel

1. CONTACT INFORMATION

School of Engineering
Brown University
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2. EDUCATION

- Ph.D. in Computer Science and Engineering, University of California, San Diego, 2001 – 2006.
  Thesis title: *New Approaches for Placement and Benchmarking of CMOS and Gene Chips*.
  Thesis advisor: Professor Andrew B. Kahng.
- M. Sc. in Electrical Engineering – Computer and Systems, Ain Shams University, Cairo, Egypt, 1998 – 2000.
  Thesis title: *Combinational Equivalence Checking*.
  Thesis advisor: Professor Ashraf Salem.
- B. Sc. (Distinction with Honors and highest GPA) in Electrical Engineering – Computer and Systems, Ain Shams University, Cairo, Egypt, 1993 – 1998.

3. RESEARCH INTERESTS

Broad interests in computer engineering areas including energy-efficient computing, design automation, embedded systems, computer architecture, reconfigurable computing and combinatorial optimization.

Current research themes:

- Energy-Efficient and Sustainable Computing
- SW/HW co-design for AI
- Molecular Computing
- Combinatorial Optimization and Machine Learning
- Design Automation

4. WORK EXPERIENCE

- **Current title:**
  - Professor of Engineering and Computer Science, Brown University.
  - Amazon Scholar.
- **Full time positions:**
  - July 2019 – : Full Professor, School of Engineering, Brown University.

- July 2021 – August 2023 : Principal Scientist at Amazon. Experience: supply chain optimization, fulfillment optimization and network planning, and machine learning for business analytics.
- July 2013 – June 2019: Associate Professor with tenure, School of Engineering, Brown University.
- July 2006 – June 2013: Assistant Professor of Engineering, Brown University.
- March 2001 – June 2006: Teaching/Research Assistant, University of California, San Diego.
- September 1998 – December 2000: Teaching/Research Assistant, Ain Shams University, Cairo, Egypt.

- **Consulting / Technical Adviser Experience:**
  - Amazon Scholar: Consulting for Amazon Supply Chain Optimization Technologies (SCOT) team.
  - Fish & Richardson law firm: Expert witness on power management patents for processors.
  - Prince Lobel Tye: Expert witness on approximate computing patents.
- **Visiting and other positions:**
  - Visiting scholar at Harvard School of Engineering and Applied Sciences (Spring 2015 sabbatical).
  - Intel Design and Technology Group, Santa Clara (Summer 2005).
  - IBM Austin Research Laboratory, Austin, Texas (Summer 2004).
  - TIMA Laboratory, Grenoble, France (Summer 2000).
  - Mentor Graphics Corporation, Cairo, Egypt (Fall 1998 – Fall 2000).

5. AWARDS AND RECOGNITIONS

2024 IEEE Transactions on Computer-Aided Design Donald O. Pederson Best Paper award.

2024 AIIA (International Artificial Intelligence Industry Alliance) Fellow.

2023 Amazon Scholar.

2023 AAIA (Asia-Pacific Artificial Intelligence Association) Fellow.

2022 IEEE Fellow (class of 2023) for Contributions to Energy-Efficient and Approximate Computing.

2020 Best Paper Nomination, VLSI SoC Symposium.

2020 Best Paper Nomination, Design Automation Test in Europe (DATE) Conference.

2018 Best Paper Award, IEEE International Green and Sustainable Computing Conference (IGSC).

2016 National Academy of Sciences (NAS) US-Arab Frontiers Fellowship.

2015 Best Paper Nomination, International Conference on Computer-Aided Design (ICCAD)

2014 Elevated to IEEE Senior status

2010 Best Paper Award, International Symposium on Low-Power Electronic Design (ISLPED) (2 out of 203 papers)

2010 DAC A. Richard Newton award (1 out of 20 proposals)

2010 National Science Foundation CAREER award

2008 Best Paper Nomination, Asian South-Pacific Design Automation Conference (ASPDAC) (10 out of 350 papers)

2008 Brown University Richard B. Salomon Award

2005 Best Paper Nomination, International Conference on Computer-Aided Design (ICCAD)

2005 First Place Award, VLSI placement contest, ACM International Symposium on Physical Design (ISPD) (1 out of 9 teams)

2005 “Hot” (most downloaded) article in Operations Research Letters

2004 Best Poster Award, UCSD Jacobs School of Engineering Research Review Expo (10 out of 200 posters)

2003 Best Poster Award, UCSD Jacobs School of Engineering Research Review Expo (10 out of 180 posters)

2002 Best Paper Award, Design Automation and Test in Europe Conference (DATE) (3 out of 476 papers)

2001 Cal-(IT)^2 fellowship, University of California, San Diego

1998 First rank of graduating class among all engineering departments, Ain Shams University, Cairo, Egypt

1993 High school valedictorian, El-Nasr English School, Cairo, Egypt

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6. PUBLICATIONS (H-INDEX = 42)

– Earlier publications coauthored with Ph.D advisor, Prof. A. B. Kahng, have their authors listed in alphabetical order.

Books

[1] S. Reda and A. N. Nowroz, "Power Modeling and Characterization of Computing Devices: A Survey," Foundations and Trends in Electronic Design Automation, NOW Publishers, 2012. `https://www.amazon.com/dp/1601985606`.

[2] S. Reda and M. Shafique (Eds), "Approximate Circuits: Methodologies and CAD", Springer, 2019 `https://www.amazon.com/dp/3319993216`.

Book Chapters

[1] Z. Yuan, S. Reda, and A. K. Coskun, "Compact Thermal Modeling of Emerging Cooling Technologies for Processors", in *Embedded Cooling of Electronic Devices*, to appear 2021.

[2] S. Dai, C. R. Tulloss, X. Lian, K. Hu, S. Reda, and J. K. Rosenstein, "Low Power Current-Mode Relaxation Oscillators for Temperature and Supply Voltage Monitoring", in *IFIP Advances in Information and Communication Technology*, pp. 25 - 44, Springe Nature, 2021.

[3] S. Hashemi and S. Reda, "Approximate Multipliers and Dividers Using Dynamic Bit Selection", in *Approximate Circuits: Methodologies and CAD*, pp. 25 - 44, Springer, 2019.

[4] S. Hashemi, H. Tann and S. Reda, "Approximate Logic Synthesis Using Boolean Matrix Factorization", in *Approximate Circuits: Methodologies and CAD*, pp. 141 - 154, Springer, 2019.

[5] H. Tann, S. Hashemi and S. Reda, "Lightweight Deep Neural Network Accelerators using Approximate SW/HW Techniques", in *Approximate Circuits: Methodologies and CAD*, pp. 289 - 305, Springer, 2019.

[6] H. Tann, S. Hashemi, F. Buttafuoco, and S. Reda, "Approximate Computing for Iris Recognition Systems", in *Approximate Circuits: Methodologies and CAD*, pp. 331 - 348, Springer, 2019.

[7] A. B. Kahng and S. Reda and Q. Wang, "APlace: A High Quality, Large-Scale Analytical Placer," *Modern Circuit Placement: Best Practices and Results*, Springer, 2007, J. Cong and G-J. Nam (ed.), pp. 163 – 187.

[8] A. B. Kahng, I. Măndoiu, S. Reda, A. Zelikovsky and X. Xu, "Computer-Aided Optimization of DNA Array Design and Manufacturing," *Design Automation Methods and Tools for Microfluidics-Based Biochips*, Springer, 2006, K. Chakrabarty (ed.), pp. 253 – 269.

[9] A. B. Kahng and S. Reda, "Digital Layout - Placement," *The CRC Handbook of EDA for IC Design*, CRC Press, 2005, G. Martin and L. Lavagno (ed.), Vol. 2., pp. 5.1 – 5.23.

Papers in Archival Proceedings and Journals

[1] A. Agiza, M. Mostagir, and S. Reda, "PoliTune: Analyzing the Impact of Data Selection and Fine-Tuning on Economic and Political Biases in Large Language Models," *Proceedings of the 2024 AAAI/ACM Conference on AI, Ethics, and Society*, 2024.

[2] **J** M. Abdelatty, J. Incandela, P. Raj, K. Hu, J. Larkin. S. Reda, J. Rosenstein, "Electrical Capacitance Tomography of Cell Cultures on a CMOS Microelectrode Array," *IEEE Transactions on Biomedical Circuits and Systems*, 2024.

[3] **J** A. Agiza, S. Marriott, J. K. Rosenstein, E. Kim, and S. Reda, "pH-Controlled Enzymatic Computing for Digital Circuits and Neural Networks." *Physical Chemistry Chemical Physics, Royal Society of Chemistry*, 2024.

[4] A. Agiza, M. Neseem, S. Reda, "MTLoRA: Low-Rank Adaptation Approach for Efficient Multi-Task Learning," *IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR)*, 2024. **Highlight paper – 2.6% of submitted papers.**

[5] M. Neseem, C. McCullough, R. Hsin, C. Leichner, S. Li, I. Chong, A. Howard, L. Lew, S. Reda, V. Rautio, D. Moro, "PikeLPN: Mitigating Overlooked Inefficiencies of Low-Precision Neural Networks," *IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR)*, 2024.

[6] S. M. Nabavinejad, S. Reda and T. Guo, "MediatorDNN: Contention Mitigation for Co-located DNN Inference Jobs," *IEEE International Conference on Cloud Computing*, 2024.

[7] M. Abdelatty, J. Incandela, K. Hu, J. Larkin. S. Reda, J. Rosenstein, "Microscale 3-D Capacitance Tomography with a CMOS Sensor Array," *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2023.

[8] J. Ma and S. Reda, "WeNet: Configurable Neural Network with Dynamic Weight-Enabling for Efficient Inference," *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2023.

[9] A. Agiza, R. Roy, T. Ene, S. Godil, S. Reda and B. Catanzaro, "GraPhSyM: Graph Physical Synthesis Model," *Proceedings of the 42nd International Conference on Computer-Aided Design (ICCAD)*, 2023.

[10] **J** A. Agiza, K. Oakley, J. K. Rosenstein, B. M. Rubenstein, E. Kim, M. Riedel and S. Reda, "Digital Circuits and Neural Networks based on Acid-Base Chemistry implemented by Robotic Fluid Handling," *Nature Communications*, 2023

[11] **J** A. Hosny, S. Reda, "Automatic MILP Solver Configuration by Learning Problem Similarities," *Annals of Operations Research*, (2023).

[12] M. Neseem, A. Agiza, S. Reda, "AdaMTL: Adaptive Input-dependent Inference for Efficient Multi-Task Learning", *Proceedings of IEEE/CVF Computer Vision and Pattern Recognition Workshops (CVPRW – ECV)*, 2023.

[13] J. Ma and S. Reda, "RUCA: RUntime Configurable Approximate Circuits with Self-Correcting Capability," *IEEE Asia and South Pacific Design Automation Conference*, 2023.

[14] S. Chetoui, R. Shah, S. Abdelaziz, A. Golas, F. Hijaz and S. Reda, " ARBench: Augmented Reality Benchmark For Mobile Devices," *IEEE Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2022.

[15] **J** S. M. Nabavinejad, S. Reda and M. Ebrahimi, "Coordinated Batching and DVFS for DNN Inference on GPU Accelerators," *IEEE Transactions on Parallel and Distributed Systems,* 2022.

[16] S. Chetoui, M. Chen, A. Golas, F. Hijaz, A. Belouchrani and S. Reda, "Alternating Blind Identification of Power Sources for Mobile SoCs," *ACM/SPEC International Conference on Performance Engineering*, 2022.

[17] **J** S. M. Nabavinejad and S. Reda, "BayesTuner: Leveraging Bayesian Optimization For DNN Inference Configuration Selection," *IEEE Computer Architecture Letters*, 2021.

[18] **J** A. Hosny and S. Reda, "Characterizing and Optimizing EDA Flows for the Cloud," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2021.

[19] A. Hosny, M. Neseem and S. Reda, "Sparse Bitmap Compression for Memory-Efficient Training on the Edge," *ACM/IEEE Symposium on Edge Computing (SEC)*, 2021.

[20] **J** Z. Yuan, P. Shukla, S. Chetoui, S. Nemtzow, S. Reda and A. Coskun, "PACT: An Extensible Parallel Thermal Simulator for Emerging Integration and Cooling Technologies", *IEEE Transactions Computer-Aided Design*, 2021.

[21] [J] S. Chetoui and S. Reda, "CasCon: Cascaded Thermal And Electrical Current Throttling for Mobile Devices", *IEEE Embedded Systems Letters*, 2021.

[22] [J] A. Dombroski, K. Oakley, C. Arcadia, F. Nouraei, S. L. Chen, C. Rose, B. Rubenstein, J. Rosenstein, S. Reda, and E. Kim, "Implementing Parallel Arithmetic via Acetylation and Its Application to Chemical Image Processing" *Royal Society of Chemistry*, 2021.

[23] [J] C. Arcadia, A. Dombroski, K. Oakley, S. L. Chen, H Tann, C. Rose, E. Kim, S. Reda, B. M. Rubenstein and J. K. Rosenstein, "Leveraging autocatalytic reactions for chemical- domain image classification Journal of Chemical Science, *Proceedings of the Royal Society A*, 2021.

[24] S. Chetoui and S. Reda, "Workload- and User-aware Battery Lifetime Management for Mobile SoCs," *IEEE/ACM Design Automation Test in Europe (DATE)*, 2021

[25] A. Hosny and S. Reda, "Characterizing and Optimizing EDA Flows for the Cloud," *IEEE/ACM Design Automation Test in Europe (DATE)*, 2021.

[26] S. M. Nabavinejad, S. Reda, M. Ebrahimi, "BatchSizer: Power-Performance Trade-off for DNN Inference," *IEEE Asian-South Pacific Design Automation Conference*, 2021.

[27] [J] J. Ma, S. Hashemi and S. Reda, "Approximate Logic Synthesis Using Boolean Matrix Factorization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2021.

[28] [J] R I. Scarabottolo, G. Ansaloni, G. Constantinides, L. Pozzi and S. Reda "Approximate Logic Synthesis: A Survey", to appear in Proc. of the IEEE, 2020

[29] S. Dai, C. Tulloss, X. Lian, K. Hu, S. Reda and J. Rosenstein, "Temperature and Supply Voltage Monitoring with Current-mode Relaxation Oscillators", to appear in *IEEE VLSI-SoC*, 2020. **best paper nominee**

[30] X. Lian, S. Reda and J. Rosenstein, "CSimultaneous Estimation of Temperature and Voltage from Digital Delay Diversity", to appear in *IEEE VLSI-SoC*, 2020.

[31] [J] R. Azimi and S. Reda, "PowerCoord: Power Capping Coordination for Multi-CPU/GPU Servers using Reinforcement Learning," to appear in *ElSevier Sustainable Computing: Informatics and Systems*, 2020.

[32] [J] J. K. Rosenstein, C. Rose, S. Reda, P. M. Weber, E. Kim, J. Sello, J. Geiser, E. Kennedy, C. Arcadia, A. Dombroski, K. Oakley, S. L. Chen, H Tann, and B. M. Rubenstein, "Principles of Information Storage in Small-Molecule Mixtures," to appear in *IEEE Transactions on NanoBioScience*, 2020.

[33] Y, Zhao, G. Vaartstra, P. Shukla, Z Lu, E. Wang, S. Reda and A. Coskun "A Learning-Based Thermal Simulation Framework for Emerging Two-Phase Cooling Technologies," to appear in ACM/IEEE Design Automation Test in Europe (**DATE**), 2020. **Best Paper Nomination**

[34] [J] S. Chetoui and S. Reda, "Coordinated Self-tuning Thermal Management Controller for Mobile Devices," to appear in *IEEE Design & Test*, 2020.

[35] M. Neseem, J. Nelson and S. Reda, "AdaSense: Adaptive Low-Power Sensing and Activity Recognition for Wearable Devices," to appear in IEEE/ACM *DAC*, 2020.

[36] M. Syed Nabavinejad, L. Mashayekhy and S. Reda, "ApproxDNN: Incentivizing DNN Approximation in Cloud," to appear in IEEE/ACM *CCGrid*, 2020.

[37] [J] K. Rajan, S. Hashemi, U. Karpuzcu, M. Doggett and S. Reda, "Dual-precision fixed-point arithmetic for low-power ray-triangle intersections," to appear in *ElSevier Computer & Graphics*, 2020.

[38] [J] C. Arcadia, E. Kennedy, J. Geiser, A. Dombroski, K. Oakley, S. L. Chen, L. Sprague, M. Ozmen, J. Sello, P. Weber, S. Reda, C. Rose, E. Kim, B. Rubenstein, and J. Rosenstein , "Multicomponent Molecular Memory," to appear in *Nature Communications*, 2020.

[39] A. Hosny, S. Hashemi, M. Shalan and S. Reda, "DRiLLS: Deep Reinforcement Learning for Logic Synthesis", in *IEEE Asia and South Pacific Design Automation Conference*, 2020.

[40] [J] M. Nabavinejad, Hassan Hafez-Kolahi and S. Reda, "Coordinated DVFS and Precision Control for Deep Neural Networks," in *IEEE Computer Architecture Letters*, 2019.

[41] [J] H. Tann, H. Zhao and S. Reda, "A Resource-Efficient Embedded Iris Recognition System Using Fully Convolutional Networks" in ACM Journal on Emerging Computing Technologies, 2019.

[42] Y, Zhao, P. Shukla, G. Vaartstra, E. Wang, S. Reda and A. Coskun "Modeling and Optimization of Chip Cooling with Two-Phase Vapor Chambers," to appear in IEEE International Symposium on Low-Power Electronics & Design (**ISLPED**), 2019.

[43] T. Ajayi, V. A. Chhabria, M. Fogaca, S. Hashemi, C. Holehouse, A. Hosny, A. B. Kahng, M. Kim, J. Lee, U. Mallappa, M. Neseem, G. Pradipta, S. Reda, M. Saligane, S. S. Sapatnekar, C. Sechen, M. Shalan, W. Swartz, L. Wang, Z. Wang, M. Woo and B. Xu, "Toward an Open-Source Digital Flow: First Learnings from the OpenROAD Project," IEEE/ACM Design Automation Conference (**DAC**), 2019.

[44] Y, Zhao, G. Vaartstra, P. Shukla, S. Reda, E. Wang and A. Coskun "Two Phase Cooling with Micropillar Evaporators: A New Approach to Remove Heat from Future High Performance Chips," to appear in IEEE iTherm, 2019.

[45] [J] F. Kaplan, M. Said, S. Reda and A. Coskun "Modeling and Optimization of Chip Cooling with Two-Phase Vapor Chambers," to appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019.

[46] S. Hashemi and S. Reda, "Generalized Matrix Factorization Techniques for Approximate Logic Synthesis," in *IEEE /ACM Design Automation & Test in Europe* (**DATE**), 2019, to appear.

[47] R. Azimi, C. Jing and S. Reda, "PowerCoord: A Coordinated Power Capping Controller for Multi-CPU/GPU Servers," to appear in *IEEE International Green and Sustainable Computing Conference* (**IGSC**), 2018. **Best Paper Award**.

[48] M. Said, S. Chetoui, A. Belouchrani and S. Reda, "Understanding the sources of power consumption in Mobile SoCs," to appear in *IEEE International Green and Sustainable Computing Conference* (**IGSC**), 2018.

[49] [J] R. Azimi, T. Fox, W. Gonzalez and S. Reda, "Scale-out vs Scale-up: A Study of ARM-based SoCs on Server-class workloads," in *Transactions on Modeling and Performance Evaluation of Computing Systems* (**TOMPECS**), 3(4), pp. 18:1-18:23, 2018.

[50] S. Hashemi, H. Tann and S. Reda, "BLASYS: Approximate Logic Circuit Synthesis Using Boolean Matrix Factorization," in *IEEE/ACM Design Automation Conference* (**DAC**), pp. 55:1-55:6, 2018.

[51] C. Arcadia, H. Tann, A. Dombroski, K. Ferguson, S. L. Chen, E. Kim, B. Rubenstein, C. Rose, S. Reda and J. Rosenstein, "Parallelized Linear Classification with Volumetric Chemical Perceptrons", in *IEEE Conference on Rebooting Computer* (**ICRC**), pp. 1-9, 2018.

[52] C. Rose, S. Reda, B. Rubenstein and J. Rosensetin, "Computing With Chemicals: Perceptrons Using Mixtures of Small Molecules", in *IEEE International Symposium on Information Theory* (**ISIT**), pp. 2236-2240, 2018.

[53] S. Hashemi, H. Tann, F. Buttafuoco and S. Reda, "Approximate Computing for Biometric Security Systems: A Case Study on Iris Scanning," in *IEEE Design, Automation Test in Europe* (**DATE**), pp. 319-324, 2018. Acceptance Rate 23.7%.

[54] M. Nabavinejad, X. Zhan, R. Azimi, M Goudarzi, and S. Reda, "QoR-Aware Power Capping for Approximate Big Data Processing," to appear in *IEEE Design, Automation Test in Europe* (**DATE**), pp. 253-256,, 2018.

[55] [J] S. Reda, K. Dev and A. Belouchrani, "Blind Identification of Thermal Models and Power Sources from Thermal Measurements," in *IEEE Journal on Sensors* (**SENSORS**), Vol. 18(2), pp. 680-691, 2018.

[56] [J] K. Dev, X. Zhan and S. Reda, "Scheduling on CPU+GPU Processors under Dynamic Conditions," in Journal on Low-Power Electronics (**JOLPE**), Vol. 13(4), pp. 551-568, American Scientific Publishers, 2017.

[57] S. Steffl and S. Reda, "LACore: A Supercomputing-Like Linear Algebra Accelerator for SoC-Based Designs," in IEEE Conference on Computer Design (**ICCD**), pp. 137-144, 2017. Acceptance rate 29%.

[58] [J] S. Reda, "3D Integration Advances Computing", **Nature**, Vol. 547, pp. 38-40, July 2017. (invited in News & Views Section)

[59] R. Azimi, T. Fox and S. Reda, "Understanding the Role of GPGPU-accelerated SoC-based ARM Clusters", in IEEE Cluster (**Cluster**), pp. 333-343, 2017. Acceptance rate 21.8%.

[60] M. Shalan and S. Reda, "CloudV: A Cloud-Based Educational Digital Design Environment," IEEE International Conference on Microelectronic Systems Education (MSE), pp. 39 - 42, 2017.

[61] F. Kaplan, S. Reda and A. Coskun, "Fast Thermal Modeling of Liquid, Thermoelectric, and Hybrid Cooling", in IEEE The Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (**iTherm**), pp. 726 – 735, 2017.

[62] H. Tann, S. Hashemi, R. I. Bahar and S. Reda, "Hardware-Software Codesign of Highly Accurate, Multiplier-free Deep Neural Networks", in *IEEE/ACM Design Automation Conference* (**DAC**), pp. 28:1-28:6, 2017.

[63] R. Azimi, M. Badiei, L. Na and S. Reda, "Fast Decentralized Power Capping for Server Clusters", *in IEEE Symposium on High-Performance Computer Architecture* (**HPCA**), pp. 181-192, , 2017. Acceptance rate 22%.

[64] S. Hashemi, N. Anthony, C. Tann, R. I. Bahar and S. Reda, "Understanding the Impact of Precision Quantization on the Accuracy and Energy of Neural Networks", in IEEE/ACM Design, Automation & Test in Europe (**DATE**), pp. 1474-1479, 2017.

[65] S. Reda and A. Belouchrani, "Blind Identification of Power Sources in Multicore Processors", in IEEE/ACM Design, Automation & Test in Europe (**DATE**), pp.1739-1744, 2017.

[66] K. Dev, X. Zhan and S. Reda, "Power-Aware Characterization and Mapping of Workloads on CPU-GPU Processors", in IEEE International Symposium on Workload Characterization (**IISWC**), pp. 225-226, 2016.

[67] **J** K. Nepal, S. Hashemi, C. Tann, R. I. Bahar and S. Reda, "Automated High-Level Generation of Low-Power Approximate Computing Circuits", in IEEE Transactions on Emerging Topics in Computing, 2016.

[68] **J** X. Zhan, R. Azimi, S. Kanev, D. Brooks and S. Reda, "CARB: A C-State Power Management Arbiter For Latency-Critical Workloads", in IEEE Computer Architecture Letters (**CAL**), 16(1): 6-9, 2016.

[69] C. Tann, S. Hashemi, R. I. Bahar and S. Reda, "Runtime Configurable Deep Neural Networks for Energy-Accuracy Trade-off", in *IEEE International Conference on Hardware/Software Codesign and System Synthesis* (**CODES**), 34:1-34:10, 2016.

[70] K. Dev and S. Reda, "Scheduling Challenges and Opportunities in Integrated CPU+GPU Processors ", in ACM/IEEE Symposium on Embedded Systems for Real-time Multimedia (**ESTI**), pp. 78-83, 2016.

[71] Ulusel, C. Picardo, C. Harris, S. Reda and R. I. Bahar, "Hardware Acceleration of Feature Detection and Description Algorithms on Low-Power Embedded Platforms", in *IEEE Field Programmable Logic* (**FPL**), pp. 1-9, 2016.

[72] K. Dev, S. Reda, I. Paul, W. Huang and W. Burleson, "Workload-aware Power Gating Design and Run-time Management for Massively Parallel GPGPUs", *in IEEE Symposium on Very-Large Scale Integration* (**ISVLSI**), pp. 242-247, 2016.

[73] S. Hashemi, R. I. Bahar and S. Reda, "A Low-Power Dynamic Divider for Approximate Applications", in *IEEE/ACM Design Automation Conference* (**DAC**), 105:1-105:6, 2016.

[74] X. Zin, M. Shoaib and S. Reda, "BXplore: Creating Soft Heterogeneity in Clusters Through BIOS Re-configuration", in *IEEE Cluster, Cloud and Grid Computing* (**CCGRID**), 540-549, 2016.

[75] M. Badiei, X. Zhan, R. Azimi, S. Reda and N. Li, "DiBA: Distributed Power Budget Allocation for Large-Scale Computing Clusters", in *IEEE Cluster, Cloud and Grid Computing* (**CCGRID**), pp. 70-79, 2016.

[76] **J** X. Zhan and S. Reda, "Power Budgeting Techniques for Data Centers", IEEE Transactions on Computers, Vol. 64(8), pp. 2267-2278, 2015.

[77] R. Azimi, X. Zhan and S. Reda, "How Good Are Low-Power 64-bit SoCs for Server-Class Workloads?," in *IEEE International Symposium on Workload Characterization* (**IISWC**), pp. 116-117, 2015.

[78] S. Hashemi, R. I. Bahar and S. Reda, "DRUM: A Dynamic Range Unbiased Multiplier for Approximate Applications," in ACM/IEEE International Conference on Computer-Aided Design, pp. 418-425, 2015. (**ICCAD**) **Best Paper Candidate (4 selected out of 382 submissions)**. Acceptance rate 24.6%.

[79] S. Jayakumar, S. Reda, "Making Sense of Thermoelectrics for Processor Thermal Management and Energy Harvesting," in *IEEE/ACM International Symposium on Low-Power Electronics and Design* (**ISLPED**), pp. 31-36, 2015. Full paper acceptance rate 19.6%.

[80] **J** A. N. Nowroz, K. Hu, F. Koushanfar, S. Reda, "Novel Techniques for High-Sensitivity Hardware Trojan Detection using Thermal and Power Maps", in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 33(12), pp.1792-1805, 2014.

[81] **J** red Ulusel, K. Nepal, R. I. Bahar and S. Reda, "Fast Design Exploration for Performance, Power and Accuracy Tradeoffs in FPGA-based Accelerators, in ACM Transactions on Reconfigurable Technology and Systems, Vol 7(1), pp. 4:1–4:22, 2014.

[82] R. Azimi, X. Zhan and S. Reda, "Thermal-aware Layout Planning for Heterogeneous Datacenters", in IEEE/ACM International Symposium on Low-Power Electronics and Design (**ISLPED**), pp. 245-250, 2014.

[83] K. Nepal, Y. Li, R. I. Bahar and S. Reda, "ABACUS: A Technique for Automated Behavioral Synthesis of Approximate Computing Circuits," in *IEEE/ACM Design, Automation and Test in Europe* (**DATE**), 2014. Acceptance rate 23.1%

[84] **J** A. Nowroz, G. Woods and S. Reda, "Power Mapping of Integrated Circuits Using AC-based Thermography," in *IEEE Transactions on Very Large Scale Integration*, Vol. 21(8), pp. 1398-1409, 2013.

[85] **J** S. Reda, A. N. Nowroz, and R. Cochran, "Post-Silicon Power Mapping Techniques for Integrated Circuits," in *ElSevier VLSI Integration*, Vol 46, pp. 69-79, 2013.

[86] K. Dev, A. N. Nowroz and S. Reda, "Power Mapping and Modeling of Multi-core Processors," in *IEEE International Symposium on Low-Power Electronics and Design* (**ISLPED**), pp. 39-44, 2013. Acceptance rate 35%.

[87] C. Hankendi, S. Reda and A. Coskun, "vCap: Adaptive Power Capping for Virtualized Servers," in *IEEE International Symposium on Low-Power Electronics and Design* (**ISLPED**), pp. 415-420, 2013. Acceptance rate 35%.

[88] X. Zhan and S. Reda, "Techniques for Energy-Efficient Power Budgeting in Data Centers," in *IEEE/ACM Design Automation Conference* (**DAC**), Article No. 176, 2013. Acceptance rate 21.7%.

[89] K. Dev, G. Woods and S. Reda, "High-Throughput TSV Testing and Characterization for 3D Integration Using Thermal Mapping," in *IEEE/ACM Design Automation Conference* (**DAC**), Article No. 73, 2013. Acceptance rate 21.7%.

[90] F. Paterna and S. Reda, "Mitigating Dark Silicon Problems Using Superlattice-based Thermoelectric Coolers," *Design, Automation and Test in Europe* (**DATE**), pp. 1391-1394, 2013. Acceptance rate 30%.

[91] K. Hu, A. Nowroz, S. Reda and F. Koushanfar, "High-Sensitivity Hardware Trojan Detection Using Multimodal Characterization Power Mapping of Integrated Circuits Using AC-based Thermography," in *Design, Automation and Test in Europe* (**DATE**), pp. 1271-1276, 2013. Acceptance rate 30%.

[92] **J** R. Cochran and S. Reda, "Thermal Prediction and Adaptive Control Through Workload Phase Detection," in ACM Transactions on Design Automation of Electronic Systems, Vol 18(1), 7:1-7:19, 2012.

[93] K. Nepal, red Ulusul, R. I. Bahar and S. Reda, "Fast Multi-Objective Algorithmic-Design Co-Exploration for FPGA-based Accelerators," *IEEE International Symposium on Field-Programmable Custom Computing Machines (***FCCM***)*, pp. 65-68, 2012.

[94] **J** S. Reda, R. Cochran and A. Coskun, "Adaptive Power Capping for Servers with Multi-Threaded Workloads," in IEEE MICRO, Vol 32(5), pp. 64-75, 2012.

[95] **J** S. Reda and A. N. Nowroz, "Power Modeling and Characterization of Computing Devices: A Survey," in Foundations and Trends in Electronic Design Automation, NOW Publishers, Vol. 6(2), pp. 121 – 216, 2012. Also available in a book format.

[96] **J** S. Reda, "Thermal and Power Characterization Techniques for Real Computing Systems," *IEEE Journal on Emerging Topics in Circuits and Systems,* Vol 1(2), pp. 76 – 87, 2011.

[97] **J** S. Reda, R. Cochran and A. N. Nowroz, "Improved Thermal Tracking for Processors Using Hard and Soft Sensor Allocation Techniques," *IEEE Transactions on Computers,* Vol. 60(6), pp. 841-861, 2011.

[98] R. Cochran, C. Hankendi, A. Coskun and S. Reda, "Pack & Cap: Adaptive DVFS and Thread Packing Under Power Caps," *IEEE/ACM International Symposium on Microarchitecture (***MICRO***)*, pp. 175-185, 2011. Acceptance rate 21%.

[99] R. Cochran, C. Hankendi, A. Coskun and S. Reda, "Identifying the Optimal Energy-Efficient Operating Points of Parallel Workloads," *ACM/IEEE International Conference on Computer-Aided Design (***ICCAD***)*, pp. 608-615, 2011. Acceptance rate 30%.

[100] A. N. Nowroz and S. Reda, "Improved Post-Silicon power Modeling Using AC Lock-In Techniques," in proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, pp. 101-106, 2011. Acceptance rate 23%.

[101] A. N. Nowroz and S. Reda, "Thermal and Power Characterization of Field-Programmable Gate Arrays," in proceedings of *ACM International Symposium on Field Programmable Gate Arrays (***FPGA***)*, pp. 111-114, 2011. Full + short paper acceptance rate 43%.

[102] **J** S. Reda and S. Nassif, "Accurate Spatial Estimation and Decomposition Techniques for Variability Characterization," *IEEE Transactions on Semiconductor Manufacturing,* 23(3), 2010, pp. 345-357.

[103] N. H. Khan, S. Reda and S. Hassoun, "Early Estimation of TSV Area for Power Delivery in 3D Integrated Circuits," in proceedings of *IEEE International 3D Systems Integration Conference (***3D-IC***)*, pp. 1–6, 2010.

[104] R. Cochran, A. Nowroz and S. Reda , "Post-Silicon Power Characterization Using Thermal Infrared Emissions," in proceedings of *ACM/IEEE International Symposium on Low-Power Electronics and Design (***ISLPED***)*, pp. 331-336, 2010. **Best Paper Award (2 out of 203 papers)**. Full paper acceptance rate 23%.

[105] A. Nowroz, R. Cochran and S. Reda, "Thermal Monitoring of Real Processors: Techniques for Sensor Allocation and Full Characterization," proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, pp. 56–61, 2010. Acceptance rate 24%.

[106] R. Cochran and S. Reda, "Consistent Runtime Thermal Prediction and Control Through Workload Phase Detection," in proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, pp. 62–67, 2010. Acceptance rate 24%.

[107] **J** S. Reda, G. Smith and L. Smith, "Maximizing the Functional Yield of Wafer-to-Wafer 3D Integration," *in IEEE Transactions on Very Large Scale Integration Systems,* 17(9), 2009, pp. 1357-1362.

[108] S. Reda, R. I. Bahar and A. Si, "Reducing the Leakage and Timing Variability of 2D ICs Using 3D ICs," in proceedings of *ACM/IEEE International Symposium on Low Power Electronics and Design (***ISLPED***)*, pp. 283–286, 2009. Acceptance rate 35%.

[109] R. Cochran and S. Reda, "Spectral Techniques for High-Resolution Thermal Characterization with Limited Sensor Data," in proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, pp. 478–483, 2009. Acceptance rate 22%.

[110] S. Reda, "Using Circuit Structural Analysis Techniques for Networks in Systems Biology," in proceedings of *ACM System Level Interconnect Prediction (***SLIP***)*, pp. 37–44, 2009. Acceptance rate 52%.

[111] R. Le, S. Reda and R. I. Bahar, "High-Performance, Cost-Effective Heterogeneous 3D FPGA Architectures," in proceedings of *ACM Great Lakes VLSI Symposium (***GLSVLSI***)*, pp. 251–256, 2009. Acceptance rate 46%.

[112] M. Kadin, S. Reda and G. Uht, "Central vs. Distributed Dynamic Thermal Management for Multi-Core Processors: Which One is Better?," in proceedings of *ACM Great Lakes VLSI Symposium (***GLSVLSI***)*, pp. 137–140, 2009. Acceptance rate 46%.

[113] S. Reda and S. Nassif, "Analyzing the Impact of Process Variations on Parametric Measurements: Novel Models and Applications," in proceedings of *IEEE Design, Automation, Test in Europe (***DATE***)*, 2009, pp. 375–380. Accepting rate 23%.

[114] **J** C. Ferri, S. Reda and R. I. Bahar, "Parameteric Yield Management of 3D ICs: Models and Strategies for Improvement," *ACM Journal on Emerging Technologies in Computing Systems. Special issue on 3D ICs.* 4(4), 2008, pp. 19:1 – 19:22.

[115] M. Kadin and S. Reda, "Frequency and Voltage Planning for Multi-Core Processors Under Thermal Constraints," in proceedings of *IEEE International Conference on Computer Design (***ICCD***)*, pp. 463 – 470, 2008. Acceptance rate 34%.

[116] M. Kadin and S. Reda, "Frequency Planning for Multi-Core Processors Under Thermal Constraints," in proceedings of *IEEE/ACM International Symposium on Low Power Electronics and Design (***ISLPED***)*, pp. 213 – 216, 2008. Acceptance rate 40%.

[117] B. Hargreaves, H. Hult and S. Reda, "Within-die Process Variations: How Accurately Can They Be Statistically Modeled?," in proceedings of *IEEE Asian South Pacific Design Automation Conference (***ASPDAC***)*, pp. 524 – 530, 2008. **Best Paper Candidate (10 out of 350 submitted papers)**. Acceptance rate 28%.

[118] C. Ferri, S. Reda and R. I. Bahar, "Strategies for Improving the Parametric Yield and Profits of 3D ICs," in proceedings of *ACM/IEEE International Conference on Computer-Aided Design (***ICCAD***)*, 2007, pp. 220 – 226. Acceptance rate 33%.

[119] A. B. Kahng, S. Reda and P. Sharma, "On-Line Adjustable Buffering for Runtime Power Reduction," in proceedings of *IEEE International Symposium on Quality Electronic Design Automation (***ISQED***)*, 2007, pp. 550 – 555. Acceptance rate 31%.

[120] **J** A. B. Kahng and S. Reda, "Zero-Change Netlist Transformations: A New Technique for Placement Benchmarking," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(12), 2006, pp. 2806 – 2819.

[121] **J** A. B. Kahng and S. Reda, "Wirelength Minimization for Min-Cut Placements via Placement Feedback," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(7), 2006, pp. 1301 – 1312.

[122] **J** C. Alpert, A. B. Kahng, G-J. Nam, S. Reda and P. Villarubia, "A Fast Hierarchical Quadratic Placement Algorithm," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(4), 2006, pp. 678 – 691.

[123] **J** A. B. Kahng and S. Reda, "New and Improved BIST Diagnosis Techniques from Combinatorial Group Theory," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(3), 2006, pp. 533 – 543.

[124] **J** A. B. Kahng, I. Măndoiu, S. Reda, A. Zelikovsky and X. Xu, "Computer-Aided Optimization of DNA Array Design and Manufacturing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(2), 2006, pp. 305 – 320.

[125] A. B. Kahng and S. Reda, "A Tale of Two Nets: Studies in Wirelength Progression in Physical Design," in proceedings of *ACM System-Level Interconnect Prediction (***SLIP***),* 2006, pp. 17 – 24.

[126] S. Reda and A. Chowdhary, "Effective Linear Programming Based Placement Methods," in proceedings of *ACM International Symposium on Physical Design (***ISPD***),* 2006, pp. 186 – 191. Acceptance rate 35%.

[127] **J** A. B. Kahng and S. Reda, "Intrinsic Shortest Path Length: A New, Accurate A Priori Wirelength Estimator," in proceedings of *ACM/IEEE International Conference on Computer-Aided Design (***ICCAD***),* 2005, pp. 173 – 180. Acceptance Rate 25%.

[128] A. B. Kahng, S. Reda and Q. Wang, "Architecture and Details of a High Quality, Large-Scale Analytical Placer," in proceedings of *ACM/IEEE International Conference on Computer-Aided Design (***ICCAD***)*, 2005, pp. 891 – 898. **Best Paper Candidate.** Acceptance Rate 25%.

[129] Y. Cheon, P-H. Ho, A. Kahng, S. Reda and Q. Wang, "Power-Aware Placement," in proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, 2005, pp. 795 – 800. Acceptance rate 24%.

[130] A. B. Kahng and S. Reda, "Evaluation of Placer Suboptimality via Zero-Change Transformations," in proceedings of *ACM International Symposium on Physical Design (***ISPD***)*, 2005, pp. 208 – 215. Acceptance rate 37%.

[131] C. Alpert, A. B. Kahng, G-J. Nam, S. Reda and P. Villarubia, "A Semi-Persistent Clustering Technique for VLSI Circuit Placement," in proceedings of *ACM International Symposium on Physical Design (***ISPD***)*, 2005, pp. 200 – 207. Acceptance rate 37%.

[132] A. B. Kahng, S. Reda and Q. Wang, "APlace: A General Analytic Placement Framework," in proceedings of *ACM International Symposium on Physical Design (***ISPD***)*, 2005, pp. 233 – 235. **Winner of the ISPD-2005 VLSI Placement Contest.**

[133] **J** A. B. Kahng and S. Reda, "Match Twice and Stitch: A New TSP Tour Construction Heuristic," *Operations Research Letters*, 2004, 32(6), pp. 449 – 509. **"Hot" (most downloaded) article in Operations Research Letters, February 2005.**

[134] **J** A. B. Kahng, I. Măndoiu, P. Pevzner, S. Reda and A. Zelikovsky, "Scalable Heuristics for Design of DNA Probe Arrays," *Journal of Computational Biology*, Vol. 11(2-3), 2004, pp. 429 – 447.

[135] A. B. Kahng and S. Reda, "Reticle Floorplanning With Guaranteed Yield for Multi-Projects Wafer," in proceedings of *IEEE International Conference on Computer Design (***ICCD***)*, 2004, pp. 106 – 110. Acceptance rate 37%.

[136] A. B. Kahng and S. Reda, "Placement Feedback: A Concept and Method for Better Min-Cut Placements," in proceedings of *ACM/IEEE. Design Automation Conference (***DAC***)*, 2004, pp. 357 – 362. Acceptance rate 25%.

[137] A. B. Kahng, I. Markov and S. Reda, "On Legalization of Row-Based Placements," in proceedings of *ACM Great Lakes VLSI Symposium (***GLSVLSI***)*, 2004, pp. 214 – 219. Acceptance rate 40%.

[138] A. B. Kahng, I. Markov and S. Reda, "Boosting: A Min-Cut Placement with Improved Signal Delay," in proceedings of *IEEE Design Automation and Test in Europe (***DATE***)*, 2004, pp. 1098 –1103. Acceptance rate 27%.

[139] A. B. Kahng and S. Reda, "Combinatorial Group Testing Methods for the BIST Diagnosis Problem," in proceedings of *IEEE Asia South Pacific Design Automation Conference (***ASPDAC***)*, 2004, pp. 113 – 116. Acceptance rate 50%.

[140] A. B. Kahng, I. Măndoiu, S. Reda, X. Xu and A. Zelikovsky, "Evaluation of Placement Techniques for DNA Probe Array Layout," in proceedings of *ACM/IEEE International Conference in Computer-Aided Design (***ICCAD***)*, 2003, pp. 262 – 269. Acceptance Rate 26%.

[141] A. B. Kahng, I. Măndoiu, S. Reda, A. Zelikovsky and X. Xu, "Design Flow Enhancements for DNA Arrays," in proceedings of *IEEE International Conference on Computer Design (***ICCD***)*, 2003, pp. 116 – 123. Acceptance rate 33.4%.

[142] A. B. Kahng, I. Măndoiu, P. Pevzner, S. Reda and A. Zelikovsky, "Engineering a Scalable Placement Heuristic for DNA Probe Arrays," in proceedings of *ACM International Conference on Research in Computational Molecular Biology (***RECOMB***)*, 2003, pp. 148 – 156. Acceptance rate 20%.

[143] A. B. Kahng, I. Măndoiu, P. Pevzner, S. Reda and A. Zelikovsky, "Border Length Minimization in DNA Array Design," in proceedings of Springer-Verlag Lecture Notes in Computer Science Series 2452, *Workshop on Algorithms in Bioinformatics (***WABI***)*, 2002, pp. 435–448.

[144] S. Reda and A. Orailoğlu, "Reducing Test Application Time through Test Data Mutation," in proceedings of *IEEE Design Automation and Test in Europe (***DATE***)*, 2002, pp. 387 – 393. **Best Paper Award (3 out of 476 papers)**. Acceptance rate 18% for full papers.

[145] S. Reda, R. Drechsler and A. Orailoğlu, "On the Relation between BDDs and SAT for Equivalence Checking," in proceedings of *IEEE International Symposium on Quality Electronic Design Automation (***ISQED***)*, 2002, pp. 394 – 399.

[146] S. Reda and A. Salem, "Combinational Equivalence Checking using Boolean Satisfiability and Binary Decision Diagrams," in proceedings of *IEEE Design Automation and Test in Europe (***DATE***)*, 2001, pp. 122 – 126. Acceptance rate 27% for full papers.

[147] S. Reda, A. Wahba, A. Salem, D. Borrione and A. Ghonaimy, "On the Use of Don't Cares during Reachability Analysis," in proceedings of *IEEE International Symposium on Circuits and Systems (***ISCAS***)*, 2001, pp. 121 – 124.

Patents

[1] S. Reda, H. Tann, S. Hashemi and R. I. Bahar, "Deep Neural Network ", U.S. Patent No 11,521,047.

[2] S. Reda, H. Tann and H. Zhao, "Iris Recognition Using Fully Convolutional Networks", U.S. Patent Application No. 16/685,690.

[3] B. Rubenstein, J. K. Rosenstein, C. Arcadia, S. L. Chen, A. Dombroski, J. D. Geiser, E. Kennedy, E. Kim, K. M. Oakley, S. Reda, C. Rose, J. K. Sello, H. Tann, P. Weber, "Methods of Chemical Computation," U.S. Patent Application No. 17/253,013.

[4] S. Reda, A. Nowroz and K. Dev, "Power Mapping and Modeling System for Integrated Circuits", *US Patent*, US20160124443A1.

[5] C. Alpert, G-J. Nam, S. Reda and P. Villarubia, "Clustering Techniques for Faster and Better Placement of VLSI Circuits," *US Patent*, US7296252.

Workshop Papers, Posters and Technical Reports

[1] A. T. Upasani, L. Buriol, S. Reda, S. Gan and A. Jotshi, "FCAM: Regionalized Inventory Aware Fullfilment Center (FC) Assignment," *Amazon Consumer Science Summit (CSS)*, 2023.

[2] S. Reda, "VirtualZip: Accurate Origin-Destination Forecasting Using Dimensionality Reduction," *Amazon Consumer Science Summit (CSS)*, 2023.

[3] S. Reda, "RASS: Resource-Aware Shipment Sampling for Transportation Planning and Simulation," *Amazon Consumer Science Summit (CSS)*, 2023.

[4] S. Reda and H. Pang, "A Substitution Recommendation System For Grocery Buying," *Amazon Machine Learning Conference (AMLC)*, 2022.

[5] S. Reda, "Accurate Geospatial Demand Sampling," *Amazon Consumer Science Summit (CSS)*, 2022.

[6] J. Mao and S. Reda, "RUCA: RUntime Configurable Approximate Circuits with Self-Correcting Capability," *IEEE Workshop on Logic Synthesis (IWLS)*, 2021.

[7] A. Agiza and S. Reda, "OpenPhySyn: An Open-Source Physical Synthesis Optimization Toolkit," *Workshop on Open-Source EDA Technology* (WOSET), 2020

[8] J. Ma, S. Hashemi and S. Reda, "Approximate Logic Synthesis Using BLASYS," Article 5, Workshop on Open-Source EDA Technology, 2019.

[9] M. Shalan and S. Reda, "Open-source SoC Workflow in Cloud V," Article 12, Workshop on Open-Source EDA Technology, 2018.

[10] S. Hashemi, A. B. Kahng, S, Reda and M. Woo, "METRICS 2.0: A Machine-Learning Based Optimization System for IC Design," Article 21, Workshop on Open-Source EDA Technology, 2018.

[11] H. Tann, S. Hashemi and S. Reda, "Flexible Deep Neural Network Processing," arXiv Technical Report 1801.07353, 2018.

[12] S. Steffl and S. Reda, "LACore: A RISC-V Based Linear Algebra Accelerator for SoC Designs", RISCV workshop, 2017.

[13] M. Shalan and S. Reda "Cloud-Based RISC-V SoC design and Co-simulation", RISCV workshop, 2017.

[14] H. Tann, S. Hashemi, R. I. Bahar and S. Reda "Hardware-Software Codesign Techniques for Deep Neural Networks" in BARC workshop 2017.

[15] S. Reda "Taking Control of On-chip Process and Thermal Variations: From Sensors and Models to Runtime Management Techniques", Design Technology Coupling workshop, 2016.

[16] S. Reda, "Energy-Efficient Nano-Scale Computing Using Approximate Circuits", National Academies of Science USA-Arab Symposium, 2016.

[17] S. Reda "New Frontiers for Infrared Sensing in Electrical and Computer Engineering", National Academies of Science USA-Arab Symposium, 2015.

[18] K. Nepal, Y. Li, R. I. Bahar and S. Reda, "Automated High-Level Synthesis of Low Power/Area Approximate Computing Circuits", Workshop on Approximate Computing Across the Stacks (WACAS), 2014.

[19] S. Reda, "Using Infrared Imaging to Improve Integrated Circuit Design", CANDE workshop 2011.

7. GRANTS

Active Grants

1. Title: **Machine Learning-based Combinatorial Optimization for Electronic Design Automation and Beyond**
   Agency & Program: NSF
   Total Amount: $600,00K
   Start Date: 06/2024
   Role: PI

2. Title: **A Binary Quantization Research for Application Specific Machine Learning inferences**
   Agency & Program: Google
   Total Amount: $50K
   Start Date: 11/2023

Role: PI

3. Title: **A SemiSynBio-II: Hybrid Biofilm Semiconductor Information Systems**
   Agency & Program: NSF
   Total Amount: $1.5M
   Start Date: 10/2020
   Role: co-PI (with J. Rosenstein, C. Rose, B. Rubenstein and J. Larkin)

Completed Grants

1. Title: **Layered Approximate Hardware Computing with Meta-Reasoning Capabilities**
   Agency & Program: DoD ARO
   Total Amount / Brown Share: $465K.
   Start Date: 9/2019
   Role: PI

2. Title: **Novel SW/HW Approximate Computing Methodologies with Case Studies on Biometric Security Systems**
   Agency & Program: NSF SHF
   Total Amount / Brown Share: $331K
   Start Date: 07/2018 - 06/2023
   Role: sole PI

3. Title: **EAGER: Synthetic Chemical-Based Information Processing**
   Agency & Program: NSF
   Total Amount / Brown Share: $300K.
   Start Date: 8/2019
   Role: PI (co-PI: B. Rubstein, J. Rosenstein, J. Rose, J. Sello, E. Kim and P. Weber)

4. Title: **Analysis of Augmented Reality Applications on Mobile SoCs**
   Agency & Program: Facebook
   Total Amount: $218K
   Start Date: 08/2020 - 07/2022.
   Role: PI

5. Title: **Modeling the Next-Generation Hybrid Cooling Systems for High-Performance Processors**
   Agency & Program: NSF CRI
   Total Amount / Brown Share: $696K / $231K
   Start date: 06/2017 - 05/2021
   Role: PI (Lead PI: A. Coskun and E. Wang)

6. Title: **Chemical CPUs: Chemical Computational Processing via Ugi Reactions**
   Agency & Program: DARPA Molecular Informatics Program
   Total Amount / Brown Share: $4.15M
   Start Date: 01/2018 - 01/2022
   Role: co-PI (PI: B. Rubstein with J. Rosenstein, J. Rose, J. Sello, E. Kim and P. Weber)

7. Title: **A Canonical Learning-Based Approach for Thermal and Power Management for SoCs**
   Agency & Program: Samsung GRO Year 3
   Total Amount: $100K.
   Start Date: 10/2019

Role: PI

8. Title: **Thermal and Power Management for SoCs with Big, Medium and Little Clusters**
   Agency & Program Samsung GRO Year 2
   Total Amount / Brown Share: $100K
   Start Date: 11/2018
   Role: Sole PI

9. Title: **Research gift**
   Agency & Program: Facebook Research Labs
   Total Amount / Brown Share: $50K – gift.
   Start Date: 11/2018
   Role: Sole PI

10. Title: **OpenROAD: Foundations and Realization of Open, Accessible Design**
    Agency & Program: DARPA IDEA Program
    Total Amount / Brown Share: $11.38M / $444K
    Start Date: 06/2018 - 07/2020
    Role: co-PI (PI: A. B. Khang at UCSD)

11. Title: **A SW/HW Sensory-Rich Monitoring System for SoC Designs**
    Agency & Program: DARPA POSH Program
    Total Amount / Brown Share: $371K
    Start Date: 06/2018 - 05/2020
    Role: PI (co-PI: J. Rosenstein)

12. Title: **Research in Energy Efficiency of Augmented Reality Headsets**
    Agency & Program: Oculus Research
    Total Amount / Brown Share: $25K – gift.
    Start Date: 02/2018
    Role: Sole PI

13. Title: **An Integrated Framework for Thermal / Power Sensing and Management**
    Agency & Program Samsung GRO Year 1.
    Total Amount / Brown Share: $100K
    Start Date: 11/2017 – 10/2018.
    Role: Sole PI

14. Title: **FPGA Implementation of Feature Extraction Algorithms for an Iris Recognition Scanner**
    Agency & Program: RI RICC with Videology
    Total Amount / Brown Share: $50K
    Start date: 2017
    Role: PI

15. Title: **Open Cloud-based Digital ASIC design Environment**
    Agency & Program: Egypt Academy of Scientific Research and Technology JESOR program
    Total Amount / Brown Share: EGP 980K / – (equivalent to $111K at the time)
    Start date: 2016
    Role: co-PI Consultant with PI M. Shalan

16. Title: **Blind Source Separation for Improved Power Characterization through Infrared Imaging**

Agency & Program: US National Academy of Science, Engineering & Medicine US-Arab Fellowship
Total Amount / Brown Share: $2.5K
Start date: 2016
Role: PI with A. Belouchrani

17. Title: **Symbiotic Power Management for Integrated CPU - GPU Platforms**
Agency & Program: NSF XPS
Total Amount / Brown Share: $316K with REU.
Start date: 2014
Role: Sole PI.

18. Title: **Automatic High-Level Synthesis of Approximate Computing Circuits**
Agency & Program: NSF SHF
Total Amount / Brown Share: $458K with REU
Start date: 2014
Role: PI (with co-PI R. I. Bahar)

19. Title: **Enabling Autonomous Flight of Drones in Complex, Unpredictable Environments**
Agency & Program: Brown Seed
Total Amount / Brown Share: $80K
Start date: 04/2014
Role: co-PI (with R. I. Bahar, J. Kellner and O. C. Jenkins)

20. Title: **Power Mapping and Modeling of a APU Using Thermal Infrared Emission Measurements**
Agency & Program: AMD Corporation
Total Amount / Brown Share: $25K
Start date: 07/2013
Role: Sole PI

21. Title: **II-NEW: A Platform to Advance Research in Energy-Efficient Computing**
Agency & Program: NSF CRI
Total Amount / Brown Share: $190K
Start date: 2013
Role: Sole PI

22. Title: **Processing of Large Wide Area Airborne Sensor Data Streams in Hardware**
Agency & Program: DoD ONR SBIR with Videology
Total Amount / Brown Share: $26K
Start date: 2012
Role: co-PI (with R. I. Bahar)

23. Title: **Power Mapping of Many-Core Processors**
Agency & Program: Intel Corporation
Amount: $85K
Start date: 07/2011
Role: Sole PI

24. Title: **Algorithmic Techniques for Post-Silicon Characterization Using Infrared Emissions**
Agency & Program: NSF SHF
Total Amount / Brown Share: $400K / $200K

Start date: 06/2011
Role: Lead PI (w. F. Koushanfar and G. Woods)

25. Title: **CAREER: Transcending the Thermal Challenges of Tera-Scale Computing**
Agency & Program: NSF CAREER
Total Amount / Brown Share: $443 with REU
Start date: 02/2010
Role: Sole PI

26. Title: **Wide Area Video Motion Blur Elimination**
Agency & Program: DARPA SBIR with ObjectVideo Inc
Total Amount / Brown Share: $180K
Start date: 03/2010
Role: co-PI (with R. I. Bahar and J. Mundy)

27. Title: **Adaptive Hot Spot Cooling for Many-Core Processors**
Agency & Program: DAC Newton Award
Total Amount / Brown Share: $24K.
Start date: 06/2010
Role: Sole PI

28. Title: **An Infrared System for Thermal-Driven Research in Computer Vision and Electronics**
Agency & Program: DoD DURIP (ARL)
Total Amount / Brown Share: $180K
Start date: 07/2009
Role: PI (with R. I. Bahar and J. Mundy)

29. Title: **Yield Optimization Techniques for 3D Integrated Circuits**
Agency & Program: Qualcomm Corporation
Total Amount / Brown Share: $25K
Start date: 05/2008
Role: Sole PI

30. Title: **ProHunter: A Platform to Accelerate Protein Identification from Mass-Spectrometry Data**
Agency & Program: Brown Salomon award
Total Amount / Brown Share: $15K
Start date: 12/2007
Role: Sole-PI

31. **Equipment Donations:**

- Altera, equivalent of $24K, 2006
- Nvidia, equivalent of $3.2K, 2015

32. **UTRA grants (each at $3.5K):**

- J. Sriram 2010
- R. Sailor 2011
- M. Baxter 2012
- J. Y. Wu 2014
- W. Gonzalez 2016
- M. Lee 2017

- J. Vexler 2017

8. INVITED TALKS AND TUTORIALS

1. Georgia Tech, AI4OPT institute, "Using Machine Learning for Combinatorial Optimization (ML4OPT): Case Studies and Research Directions," 2/9/2024.
2. TILOS Seminar, UCSD, "How to use Machine Learning for Combinatorial Optimization?," 2022-07-20.
3. Design Automation Conference panel, "Approximate Synthesis: State-of-the-art and Future Directions", 2022.
4. Amazon, "How to Use Machine Learning for Combinatorial Optimization? Research Directions and Case Studies", 06/17/2021.
5. UC, Santa Cruz, "Energy-Efficient Design for Adaptive Approximate Computing," 03/02/2021.
6. ISAT/DARPA Energy Resilient Systems Workshop (EGRESS); "Workload Power Trends and Power Resilience", 20/1/2021.
7. VLSI-DAT, "Overview of the OpenROAD Digital Design Flow from RTL to GDS", 8/12/2020.
8. Air Force Studies Board Workshop, "Energy-Efficient Embedded Systems for Data-Rich Processing", 4/28/2020.
9. Facebook Labs, "Embedded Low-Power Processing: Ray Tracing and Neural Networks", Host: M. Doggett, 8/26/2019.
10. Quo Vadis, Logic Synthesis Workshop, "Systematic Approaches to Approximate Logic Synthesis," Florence, Italy, 3/29/2019.
11. Tufts University, "From milliWatts to megaWatts: Power Characterization and Control Techniques for Computing Systems", Boston MA, 3/15/2018.
12. The Ohio State University, "Energy Efficient Approximate Computing with Case Studies in Deep Learning and Biometric Security," Columbus, OH, 3/8/2018.
13. Samsung SARC, "An Integrated Framework for Thermal / Power Sensing and Management", Austin, TX, 10/22/2018.
14. Oculus Research, Facebook "Design of Resource-Efficient Hardware Accelerators," Seattle, WA, M. Douggett, 6/21/2018.
15. Samsung SARC Symposium, "Runtime Techniques for Thermal/Power Modeling and Management", Austin, TX, 10/17/2017.
16. Tufts University, "Energy-Efficient Approximate Computing", Medford, MA, 9/20/2017.
17. Samsung SARC, "Techniques for Thermal and Power Characterization and Modeling of Integrated Circuits", Austin, TX, 6/20/2017.
18. University of Rochester, "Energy-Efficient Approximate Computing", Rochester, NY, 3/16/2017.
19. WPI, "Energy-Efficient Approximate Computing: From Circuits to Systems", Worcester, MA, 1/1/2017.
20. NIST, "New Directions for Energy-Efficient Computing Systems: From Power Measurement to Control", Colorado, Boulder, 1/17/2017.
21. ICCAD Panel on Challenges and Opportunities of Stochastic Computing in the Dusk of Moore's Law and the Dawn of Big Data, "Approximate Accelerator Design", ICCAD, Nov 8, 2016.
22. Masdar Institute, "Energy-Efficient Nano-Scale Computing Using Approximate Circuits", National Academy of Sciences Arab-American Frontiers Symposium, 11/6/16.
23. ETSI Media Workshop, "Scheduling Challenges and Opportunities in Integrated CPU+GPU Processors", Oct 7, 2016.
24. Google Hardware Platform Engineering, "New Techniques for Power Capping and Management for Datacenters", Sept 12 2016.
25. System Design for Cloud Services Workshop, "Optimal Decentralized Power Management for Large-Scale Computing Clusters", Microsoft Faculty Summit, July 15 2016.

26. Keynote Speaker, Design Technology Workshop, "Taking Control of On-chip Process and Thermal Variations: From Sensors and Models to Runtime Management Techniques", University of Munich. 6/29/16.

27. Infineon Semiconductors, "Reducing the Cost of Variability Sensing," Munich. 6/29/16.

28. ARL, "New Directions for Energy-Efficient Computing", Army Research Lab, Aberdeen, MD. 3/1/16.

29. KAUST, "New Frontiers for Infrared Sensing for Electrical and Computer Engineering", National Academy of Sciences Arab-American Frontiers Symposium, 12/5/15.

30. Microsoft Research, "Dealing with the Performance and Power Challenges of Data Centers," 3/21/14.

31. AMD Research, "How Hot is Your Hot Chip? And How to Deal with It?," 7/22/13.

32. DAC tutorial, "Avoiding Core Meltdown! - Adaptive Techniques for Power and Thermal Management of Multi-Core Processors," 6/3/13.

33. University of California, Los Angeles, "Re-thinking Power Characterization and Management Techniques for Computing Systems," 7/27/12.

34. CMOS Emerging Technologies Conference "Addressing the Thermal Challenges in Emerging Computing Platforms", 7/18/12.

35. Tutorial in International Green Computing Conference, "Thermal Imaging and Sensing", 6/8/12.

36. University of Virginia, "Re-thinking Power Characterization and Management Techniques for Computing Systems", 4/27/12.

37. University of Illinois, Chicago, "Re-thinking Power Characterization and Management Techniques for Computing Systems", 4/20/12.

38. University of California, Berkeley, "Rethinking Power Characterization Techniques of Integrated Circuits", 2/10/12.

39. University of Minnesota, Twin Cities, "From milliWatts to megaWatts: Re-thinking Power Characterization and Management Techniques for Computing Systems", 12/13/11.

40. The CANDE (Computer-Aided Network DEsign) workshop, San Jose, "Using Infrared Imaging to Improve Integrated Circuit Design," 11/10/11.

41. Qualcomm corporation, San Diego, "Rethinking Power Characterization Techniques of Computing Devices," 6/1/11.

42. University of California, San Diego, CSE seminar "Rethinking Power Characterization Techniques of Computing Devices," 6/1/11.

43. Intel Corporation, Portland, "Rethinking Power Characterization Techniques of Computing Devices," 2/16/11.

44. Boston University, ECE seminar, "Addressing the Thermal and Power Challenges of Tera-Scale Computing," 12/8/10.

45. Columbia University, CISL EE seminar, "Addressing the Thermal and Power Challenges of Tera-Scale Computing," 12/3/10.

46. IBM T. J. Watson Research Center, Yorktown, "New Approaches for Thermal and Power Characterization," 10/27/10.

47. Harvard University EE seminar series, "Addressing the Thermal and Power Challenges of Tera-Scale Computing," 10/22/10.

48. Qualcomm Corporation, San Diego, "Thermal Characterization and Post-Silicon Power Validation: Techniques and Experimental Setup," 7/6/10.

49. Waseda University, Tokyo, "Thermal Management Solutions for Tera-Scale Computing," 9/7/09.

50. Qualcomm Corporation, San Diego, "Models for Variability Characterization and Yield Improvement for Planar and 3D ICs," 8/20/09.

51. National Tsing Hua University, Hsinchu City, Taiwan, "Yield Improvement Techniques for 3D IC Technology," 9/9/08.

52. Freescale Semiconductor Corporation, Austin TX, "Yield Improvement Techniques for 3D IC Technology," 8/26/08.

53. IBM Austin Research Lab, Austin, TX, "How Accurate Can Process Variations be Statistically Modeled and Analyzed?," 8/25/08.
54. Intel Corporation, Bangalore, "3D IC Technology: Opportunities and Challenges," 8/13/08.
55. University of California, Los Angeles, "Accurate Extraction and Statistical Modeling of Within-die Process Variations," 6/4/08.
56. University of Rhode Island, "Maximizing the Physical Performance of Multi-Core Processors Under Thermal Constraints," 6/2/08.
57. Seoul National University, "Economic Acceleration in SoC Designs Using Hardware Libraries," 9/8/07.
58. Qualcomm Corporation, San Diego, "Addressing the Challenges of Process Variations Modeling and Yield Improvement in 3D Integrated Circuits," 8/2/07.
59. Tufts University, Massachusetts, "VLSI Interconnects: Realistic Benchmarking of Optimizations and Accurate Estimation of Characteristics," 10/5/06.
60. Iowa State University, "From VLSI Circuits to Gene Chips: New Approaches to Placement and Benchmarking," 4/17/06.
61. Boston University, "From VLSI Circuits to Gene Chips: New Approaches to Placement and Benchmarking," 3/22/06.
62. Brown University, "From VLSI Circuits to Gene Chips: New Approaches to Placement and Benchmarking," 3/21/06.
63. UC, Riverside, "From VLSI Circuits to Gene Chips: New Approaches to Placement Benchmarking," 3/10/06.
64. UC, Santa Cruz, "From VLSI Circuits to Gene Chips: New Approaches to Placement Benchmarking," 2/15/06.

9. OPEN-SOURCE RESEARCH SOFTWARE/ARTIFACT RELEASES

All releases are available at `http://scale.engin.brown.edu/tools/` and `http://github.com/scale-lab`.

- **OpenPhySyn:** A tool for physical synthesis of logic circuits.
- **DRILLS:** A tool for automatic logic synthesis scripting.
- **OpenROAD:** A full RTL-GDS digital design flow
- **BLASYS:** A tool for approximate logic synthesis.
- **CloudV:** A cloud service (`http://cloudv.io`) for IC design based on open-source EDA tools.
- **LACore:** LACore is a linear algebra accelerator for RISC-V ecosystem.
- **ClusterSoCBench:** A parallel benchmark set to evaluate clusters made of SoC ARM processors.
- **BPI:** A blind power identification software for processors.
- **DPC:** A software tool for decentralized power capping of computing clusters.
- **ABACUS:** ABACUS is a high-level synthesis tool for approximate computing circuits.
- **DRUM:** HDL for an approximate multiplier with a dynamic range and unbiased error distribution.

10. MENTORING AND ADVISING

Current Research Group Members:

1. Abdelrahman Ibrahim (CS PhD program, Fall 2018 – Expected August 2023)
2. Marina Neseem (ECE PhD program, Fall 2019 –)
3. Ahmed Agiza (CS PhD program, Fall 2019 –)

4. Jingxiao Ma (CS ScM program, Fall 2020 –)

5. Manar Abdelatty (ECE PhD program, Spring 2022 –)

Supervised Completed PhD Theses:

1. Ryan J. Cochran, Ph.D. (2008 – 2012). First job position at Qualcomm.
   Thesis Title: "Techniques for Adaptive Power and Thermal Sensing and Management of Multi-core Processors".

2. Nowroz Abdullah, Ph.D. (2009 – 2013). First job position at Intel.
   Thesis Title: "Power Mapping of Computing Devices: Fundamentals and Applications".

3. Kumud Nepal, Ph.D. (2010 – 2015). Co-advised with R. I. Bahar. First job position at Oracle.
   Thesis Title: "New Directions for Design-Space Exploration of Low-Power Hardware Accelerators".

4. Kapil Dev, Ph.D. (2011 – 2016). First job position at Nvidia.
   Thesis Title: "New Techniques for Power-Efficient CPU-GPU Processors"

5. Xin Zhan, Ph.D. (2012 – 2017). First job position at Apple.
   Thesis Title "Energy-Efficiency Optimization Techniques for Computing Clusters: Exploiting the Heterogeneities".

6. Soheil Hashemi, Ph.D (2013 – 2018). First position at Fathom.
   Thesis title "Approximate Computing Techniques for Accuracy Energy Trade-offs".

7. Reza Azimi, Ph.D. (2013 – 2018). First job position at Apple.
   Thesis title "Improving the Performance of Power Constrained Computing Clusters".

8. Hokchhay Tann, Ph.D. (2014 – 2019). First job position at ARM Research.
   Thesis title "Hardware-Software Co-Design of Deep Neural Network Accelerators".

9. Sofiane Chetoui, Ph.D. (2017 – 2022). First job at Nvidia.
   Thesis title "Thermal and Power Sensing and Management for Mobile System-On-a-Chip".

10. Abdelrahman Hosny, Ph.D. (2018 – 2023). First job position at Apple.
    Thesis title "Machine Learning Methods for Combinatorial Optimization."

11. Marina Neseem, Ph.D. (2019 – 2024). First job position at Nvidia.
    Thesis title "Approximate Computing Techniques: From Logic Synthesis to Deep Learning."

12. Jingxiao, Ph.D. (2019 – 2024).
    Thesis title "Machine Learning Methods for Combinatorial Optimization."

13. Ahmed Agiza, Ph.D. (2019 – 2024). First job position at Meta.
    Thesis title "Optimizing Machine Learning Models through Parameter-Efficiency."

Supervised Completed ScM Students (thesis and projects):

1. Jingxiao Ma, Sc.M. (CS project: Approximate Logic Synthesis Using Boolean Matrix Factorization), 2019 – 2020.

2. Heng Zhao, Sc.M. (project: SW/HW co-design of iris recognition systems), 2018 – 2019.

3. Shuchen Zheng, Sc.M. (2015 – 2016).
   Thesis Title: "Maximizing the performance of Parallel Applications on Heterogeneous CPU-FPGA System". First position at Facebook.

4. Kuiyuan Mao (Spring 2014)), project: synthesis of approximate circuits.

5. Yueting Li (Spring 2013), project: synthesis of approximate circuits.

6. Roto Le (Fall 2008, Spring 2009), project: design of 3D ICs.

7. Chakanetsa Zaraniyka (Fall 2008), project: modeling of process variability in CNT.

8. Brendan Hargreaves (Spring 2008), project: characterization of process variability in FPGAs.

Supervised Postdocs / visiting PhDs:

- Francesco Paterna (7/2012–12/2012).
- Morteza Nabavi Nejad (12/2016–5/2017)
- Chao Jing (10/2017 – 10/2018)
- Mostafa Said Abdelrehim (10/2017 – 12/2018)
- Soheil Hashemi (06/2018 – 05/2019)

Supervised Undergraduate Honors Theses:

- Thesis advisor for Jason Ho 2022.
  Thesis title: "Tools for Understanding Computational Behaviors of Bacterial Biofilms".
- Thesis advisor for Andrew Duncombe 2021.
  Thesis title: "ASPENN: Approximate Spike Encoding Neural Networks"
- Thesis advisor for Jon Nelson 2020.
  Thesis title: "Robust Gait Recognition Techniques for Wearable Devices".
- Thesis advisor for Krishna Rajan 2019.
  Thesis title: "Design of Low Power Ray Triangle Intersection Accelerators".
- Thesis advisor for Samuel Steffl 2017.
  Thesis title: "LACore: A Large-Format Vector Accelerator for Linear Algebra Applications".
- Thesis advisor for Tyler Fox 2017.
  Thesis title: "Revisiting The Case of ARM SoCs for High-Performance Computing Clusters".
- Thesis advisor for Sriram Jayakumar 2013.
  Thesis title: "Dynamic Thermal Management for Processors Using Thermoelectric Coolers".
- Thesis advisor for Natalie Serrino 2012.
  Thesis title: "Soft Power Capping for Improved Performance of Computing Systems".
- Thesis advisor for Shi-Qing Poh 2010.
  Thesis title: "Thermal Measurements and Characterizations for Real Processors".
- Thesis advisor for Michael Kadin 2008.
  Thesis title: "Performance Driven Frequency/Voltage Planning for Multi-Core Processors with Thermal Constraints".
- Thesis advisor for Aaron Mandle 2008.
  Thesis title: "FPGA Based Hardware Acceleration: A Case Study in Protein Identification".
- Thesis advisor for David Meisner 2007.
  Thesis title: "Design of a Shared Hardware Library for Multi-Core Environments in FPGA Fabrics".

Undergraduate Research Advising:

- Jason Ho (Summer 2021 – Spring 2022)
- Andrew Duncombe (Summer 2020 – Spring 2021)
- Jon Nelson (Summer 2019 – Spring 2020)
- Krishna Rajan (Fall 2018 and Spring 2019)
- Jake Saferstein (Fall 2018)
- Samuel Oliphant (Summer 2017)
- Myungjin Lee (Summer 2017)
- Jonathan Vexler (Summer 2017)
- Samuel Steffl (Fall 2016 and Spring 2017)

- Tyler Fox (Summer 2016, Fall 2016 and Spring 2017)
- Nicholas Anthony (Summer 2016)
- Wendy Gonzalez (Summer and Fall 2016, Spring 2018)
- Lucas Salla Pagnan (Spring 2016)
- Abdul Tabish (Spring 2016).
- Adam Cooper (Summer 2015).
- Casey Meehan (Fall 2013).
- Jie Ying Wu (Summer - Fall 2013).
- Sriram Jayakumar (Summer 2010 / Brown UTRA, Spring 2012, Spring 2013).
- Margaret Baxter (Summer 2012 Brown UTRA – Undergraduate Teaching and Research Awards)
- Patipan Prasertsom (Spring 2012)
- Natalie Serrino (Summer 2011 – Spring 2012)
- Stefan Angelevski (Summer 2011 – Spring 2012)
- Ryan Sailor (Summer 2011 – Brown UTRA)
- Patrick Temple (Summer 2010 – Spring 2011 / NSF REU – Spring 2012).
- Shi-Qing Poh (Spring 2009 – Spring 2010).
- Aung Si (Summer 2008 – Summer 2009).
- Bryant Mairs (Spring 2008).
- Aaron Mandle (Spring 2008).
- Michael Kadin (Summer 2007 – Spring 2008).
- David Meisner (Spring 2007).

PhD thesis committee:

- C. Ferri (Brown University).
- Y. Shi (Brown University).
- J. Gaudette (Brown University).
- D. Papagiannopoulou (Brown University).
- O. Uluel (Brown University).
- F. Paterna (University of Bologna).
- H. Chen (Boston University).
- C. Hankendi (Boston University).
- F. Kaplan ((Boston University).
- M. Martins (Brown University).
- C. Heelan (Brown University).
- S. Dai (Brown University).
- C. Arcadia (Brown University).

- Zihao Yuan (Boston University).

PRIME program advising: A. Rossi, B. Agma and A. Rathi.

Freshmen and sophomore advising: advisor for numerous freshmen and sophomore students.

Outreach advising:

- Research advisor for Allison Paul from Lasalle High School Academy (summer 2012 – Spring 2013).
- Research advisor for Christopher Chedid from Dartmouth High School Academy (summer 2016).

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11. COURSES

– Teaching assistant for courses in computer architecture (UCSD), compiler design (Ain Shams University), introduction to programming languages (Ain Shams University), and computing circuit design (Ain Shams University).

Semester	Class	Level	Enrollment	Plan	Lecture	HWs/Labs	Helpfulness	Average
Spring 2011*	EN164	undergraduate	37	4.56	4.60	4.36	4.88	4.60/5.00
Spring 2010*	EN52†	undergraduate	80	4.31	4.29	4.12	4.21	4.23/5.00
Spring 2009*	EN52†	undergraduate	89	4.10	4.14	3.89	4.06	4.05/5.00
Fall 2009*	EN2911X	graduate	6	4.16	4.33	4.33	4.83	4.41/5.00
Spring 2008*	EN160	undergraduate	8	4.40	4.40	4.40	4.80	4.50/5.00
Fall 2008*	EN2911C	graduate	7	3.50	3.33	3.00	3.83	3.41/5.00
Spring 2007*	EN160	undergraduate	8	4.43	4.43	4.00	5.00	4.46/5.00
Fall 2007*	EN2911X	graduate	11	4.63	4.27	4.72	4.45	4.52/5.00
Fall 2006*	EN291S40	graduate	5	4.60	4.60	4.60	5.00	4.45/5.00

Table 2: Class evaluations 2006 – 2012. scale: 5.00 (best) – 1.00. †class co-taught with H. Silverman. *

Semester	Class	Enrollment	effectiveness of instructor
Spring 2019	ENGN1640 Design of Computing Systems	15	1.10
Fall 2018	ENGN 00031 Honors Introduction to Engineering†	41	1.22/1.43
Fall 2017	ENGN 00031 Honors Introduction to Engineering†	41	1.38/1.58
Spring 2017	ENGN1640 Design of Computing Systems	16	1.00
Fall 2016	ENGN 00031 Honors Introduction to Engineering†	39	1.93/2.07
Spring 2016	ENGN1640 Design of Computing Systems	14	1.38
Fall 2015	ENGN 2910A Advanced Computer Architecture	6	1.33
Fall 2014	ENGN 2911X Reconfigurable Computing	23	1.33
Spring 2014	ENGN1640 Design of Computing Systems	18	1.20
Fall 2013	ENGN 2910A Advanced Computer Architecture	12	1.17
Fall 2012	ENGN 2911X Reconfigurable Computing	17	1.31
Spring 2012	ENGN1640 Design of Computing Systems	14	1.33

Table 3: Class evaluations 2012 – present. Scale: 1.00 (best) – 5.0. †class co-taught C. Briant in 2016 and K. S. Kim in 2017 and 2018.

12. BROWN UNIVERSITY SERVICE

- Honors Program Co-chair (Fall '18 – present)
- Affirmative Action Representative (Fall '15 – Spring '18)
- Research Advisory Board (Fall'15 – Spring '18)
- Reviewer for Salomon grants (2015 round)
- Director of Graduate Studies, School of Engineering (Fall '14)
- Faculty Mentor for Assistant Professors (S. Tellex in Computer Science)
- Electrical Sciences and Computer Engineer graduate representative (Fall '12 – Spring '14)
- Member of the committee on core Engineering education (Fall '13)
- Member of the University committee on Master Education (Fall '13)
- Honors program co-chair (Fall '12 – Spring '13)
- Undergraduate fellowship advisor (Fall'12 and Fall '13). Secured NIST fellowships for four undergraduate students.
- Member of Computer Engineering Hiring Committee, 2011 - 2012 and 2010 - 2011.
- Freshmen and sophomore concentration fair advisor 2011.
- Discussion leader in OSP BEARCORE event 2011.
- Preparation (with R.I. Bahar and D. Pacifici) of the graduate brochures of the ESCE group 2011.
- Coordinator of the Computer Engineering Advisory board 2010.
- Vice Chair of Brown University Computing Advisory board (CAB / ITAB) Fall 2008 and Spring 2009.
- Member of Brown University Computing Advisory board (CAB / ITAB) Spring 2008, Fall 2008, Spring 2009, and Fall 2009.
- Member of Brown University Information Technology Project Review Committee (ITPRC) Fall 2008 and Spring 2009.
- Seminar organizer for the School of Engineering, 2009 – 2011.
- Advisor for IEEE Chapter at Brown University, 2009 – 2011.
- Freshmen/sophomore year advisor for academic years 2008 – 2011.
- Co-organizer for the 2008 ABET accreditation of the computer engineering program.
- Mentor for students in the Program on Innovation Management and Entrepreneurship Engineering (PRIME) 2007, 2008.

13. SERVICE TO PROFESSION

- Chair:
  - General co-Chair for ACM/IEEE International Symposium on Low-Power Electronics and Design, 2021.
  - Technical Program co-Chair for ACM/IEEE International Symposium on Low-Power Electronics and Design, 2020.
  - Guest editor for IEEE Design & Test Special issue on Open-Source EDA Tools.
  - Co-founder and co-chair for the Workshop on Open-Source EDA Technology (WOSET) 2018, 2019.
  - Financial chair for IEEE Great Lakes VLSI Symposium 2016.
  - Local Arrangements Chair, IEEE International Symposium on Workload Characterization (IIWSC) 2016.
  - General Chair for IEEE System Level Interconnect Prediction (SLIP) Workshop 2010

  - Technical Program Chair for IEEE System Level Interconnect Prediction (SLIP) Workshop 2009
  - Publicity Chair for IEEE System Level Interconnect Prediction (SLIP) Workshop 2007 – 2008

- Technical Program Committee Member:
  - IEEE Symposium on Low Power Electronics and Design (ISLPED), 2017 – 2019.
  - IEEE International Symposium on Computer Architecture (External PC), 2017.
  - IEEE International Symposium on Workload Characterization, 2016, 2018.
  - IEEE International Symposium on Physical Design (ISPD) 2014, 2015, 2016.
  - IEEE/ACM Design Automation Conference (DAC) 2011 – 2013 and 2017 – 2019. DAC 2012, 2013 best paper selection committee
  - IEEE Design, Automation and Test in Europe (DATE) 2011, 2012. DATE '2018 best paper selection committee.
  - IEEE International Conference on Computer Design (ICCD) 2010 – 2016
  - IEEE International Conference on VLSI Design 2010 – 2011
  - IEEE International Conference on Very Large Scale Integration (VLSI) SoC 2011, 2012, 2014
  - IEEE Asian and South Pacific Design Automation Conference (ASP-DAC) 2008 – 2010
  - ACM/IEEE International Conference on Computer-Aided Design (ICCAD) 2008 – 2011 and 2017 – 2019. Sub-committee chair 2010-2011, best paper selection committee, 2016-2017.
  - IEEE Great Lakes VLSI Symposium (GLSVLSI) 2007 – 2008
  - IEEE International Design and Test (IDT) Workshop 2009 – 2010
  - IEEE System Level Interconnect Prediction Workshop (SLIP) 2007 – 2010
  - IEEE International Symposium on Defect and Fault Tolerance (DFT) in VLSI and Nanotechnology Systems 2015, 2016.

- Proposal Reviews:
  - National Science Foundation Panels: May 2008, Nov 2009, June 2012, February 2013, February 2016, March 2018, April 2019, Feb 2020.
  - Ralph E. Powe Junior Faculty Award review for Texas A&M University, 2017.
  - University of Texas, San Antonio, 2016.
  - Brown University Salomon Proposals 2015.
  - Canada's NSERC, 2013.
  - Czech Science Foundation, 2020.
  - Autonomous Province of Bolzano, Italy 2012.
  - Davidson Institute for Talent Development 2010.

- ACM Outstanding PhD Dissertation Award committee, 2015

- Panelist in IEEE senior member review panel (Providence, RI 6/14/2014).

- IEEE Fellow Evaluation Committee 2023.

- Associate Editor
  - ElSevier, Integration, VLSI Journal (2011 – 2019)
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (2016 – 2022)
  - ASP Journal on Low Power Electronics
  - Guest Editor for special issue of IEEE Design and Test

- Reviewer for Conferences and Journals:
  - Nature
  - IEEE Solid-State Circuits Letters

  - IEEE Computer Architecture Letters.
  - IEEE Transactions on Cloud Computing
  - IEEE Transactions on Components, Packaging and Manufacturing Technology
  - IEEE Transactions on Electron Devices
  - IEEE Transactions on Signal Processing
  - IEEE Design & Test Magazine
  - IEEE Transactions on Nanobioscience
  - IEEE Transactions on Transactions on Information Forensics & Security
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits
  - IEEE Transactions on Computers
  - IEEE Transactions on Signal Processing
  - IEEE Design and Test of Computers
  - IEEE Journal on Emerging Topics in Circuits and Systems
  - IEEE Transactions on Very Large Scale Integration
  - IEEE Transactions on Circuits and Systems
  - IEEE Transactions on Parallel and Distributed Systems
  - IEEE Transactions on Semiconductor Manufacturing
  - IEEE Transactions on Multi-Scale Computing Systems
  - Communications of the ACM
  - ACM Transactions on Design Automation of Electronic Systems
  - ACM Transactions on Embedded Computing Systems
  - ACM Journal of Emerging Technologies in Computing
  - ACM Transactions on Architecture and Code Optimization
  - Japan's IEICE journal
  - IET Circuits, Devices & Systems
  - Elsevier Integration: The VLSI Journal
  - Springer Arabian Journal for Science and Engineering
  - Kuwait Journal of Science and Engineering
  - Journal of Universal Computer Science
  - Springer Journal of Computational Electronics
  - International Conference on Computer-Aided Design
  - Design Automation Conference
  - International Symposium on Physical Design
  - International On-Line Test Workshop
  - International Conference on Computer Design
  - System Level Interconnect Prediction Workshop
  - Asian and South Pacific Design Automation Conference
  - International Symposium on Circuits and Systems
  - VLSI Test Symposium
  - International Symposium on Computer Architecture
  - Amazon Machine Learning Conference
- Contributor to ACM SIGDA Newsletter
- Member of IEEE CEDA Council
- Fellow of the Institute of Electrical and Electronic Engineers (IEEE)
- Member of the Association for Computing Machinery (ACM)