

FRANCO P. PREPARATA

Present Position

An Wang Professor of Computer Science, Brown University, 1991-

Education

1959 Dr. Ing. Electrical Engineering, University of Rome, Italy

1959–1960 Post-doctoral fellowship, Consiglio Nazionale delle Ricerche, Rome

Experience-Academic

University of Rome

1961–1965 University of Rome, Italy–Assistant Professor to the Chair of Electronic Computers, Department of Electronic Engineering

University of Illinois at Urbana

1965–1966 Research Associate in the Coordinated Science Laboratory

1966–1968 Assistant Professor of Electrical Engineering and Research Assistant Professor, Coordinated Science Laboratory

1968–1970 Associate Professor of Electrical Engineering and Research Associate Professor, Coordinated Science Laboratory

1970–1990 Professor of Electrical Engineering, of Computer Science, and Research Professor, Coordinated Science Laboratory

Other Institutions

Summer 1966 Guest Researcher, Universidad Nacional Autonoma de Mexico

Fall 1969 Visiting Professor, Institute di Elaborazione dell' Informazione, Pisa, Italy

Spring 1970 Visiting Associate Professor of Electrical Engineering, University of Texas at Austin

1972–1974 Professor of Information Sciences, University of Pisa, Italy

Spring 1979 Visiting Professor, I.R.I.A., Paris, France

Oct. 1981 Visiting Professor, Huazhong Institute of Technology, Wuhan, Hubei, China

Summer 1984 Visiting Professor, NW Telecommunication Engineering University, Xian, Shaanxi, China

Summer 1985 Visiting Professor, University of Saarland, Saarbrücken, Germany

Spring 1987 Visiting Professor, Ecole Normale Superieure, Paris, France

Summer 1988 Visiting Professor, Ecole Normale Superieure, Paris, France

Summer 1989 Visiting Professor, Ecole Normale Superieure, Paris, France

Summer 1990 Ministere-de-la-Recherche Visiting Professor, I.N.R.I.A., Sophia Antipolis, France

Summer 1992 Visiting Professor, Ecole Normale Superieure, Paris, France

Fall 1994 Visiting Professor, University of Kyoto, Kyoto, Japan
Summer 1996 Visiting Professor, Academia Sinica, Nankang, Taiwan
Spring 2002 Visiting Professor, University of Padova, Italy.
2002- (Adjunct Professorship) Kwan Im Thong Visiting Professor, School of Computing, National

Academic Recognition

1969 Libera Docenza, Italian University System

Other Recognitions

1978 Fellow, Institute of Electrical and Electronics Engineers
1993 Darlington Prize, IEEE Circuits and Systems Society
1994 Fellow of the Japan Society for the Promotion of Science
1994 Fellow of the Association for Computing Machinery
1997 Laurea Honoris Causa (honorary doctorate), University of Padova, Italy

Listing in: American Men and Women of Science

Who's Who in the Midwest

Who's Who in America

Who's Who in American Education

Who's Who in the World (6th Edition)

Who's Who in Technology

International Who's Who in Engineering

Experience-Industrial

1960-1963 Univac - Division of Sperry Rand Corporation, Rome, Italy. In charge of application and system analysis, equipment modification and installation, with responsibility for Central and Southern Italy (Technical Manager, 1961-63).

1963-1965 Selenia-S.p.A (Raytheon), Rome, Italy. Senior System Designer Responsible for the development of a special purpose digital computer for an Electromagnetic Intelligence System. Consulting for application of coding theory concepts to signal design and jamming-protected communication links.

Experience-Consulting

1972-1976 Telettra S.p.A., Milan, Italy, on digital communication problems

1973-1975 Selenia, S.p.A., Rome, Italy, on signal processing systems and fault tolerant computer design

1981-1983 IBM Corporation, on placement and routing techniques

1985 Schlumberger Corp., on computational geometry

1987-1991 Army Night Vision Laboratory, on geometric recognition

Experience-Professional-Service

- 1967-1971 Officer, IEEE Group on Information Theory, Greater Chicago Area Chapter,
(Secretary, Treasurer, Vice Chairman, Chairman)
- 1975 Scientific Director, C.I.M.E. International Summer School on Theoretical Computer
Science
- 1977 Co-chairman, 15th Annual Allerton Conference on Communications, Control and
Computing, October 1977.
- 1978 Scientific Director, Highly Specialized Seminar “Trends on Computational
Complexity,” E. Majorana Center, Erice, Italy, January 2-10, 1978.
- 1979 Scientific Director, NSF-CISM International School on “Computational Complexity,”
Udine, Italy, June 12-21, 1979.
- 1979 Co-chairman, 17th Annual Allerton Conference on Communications, Control and
Computing, October 1979.
- 1988 Director, I.R.S.T. International School on “Parallel and VLSI Algorithms,”
Trento, Italy, July 1988.
- 1990 Program Chair, ACM Symposium on Parallel Algorithms and Architecture,
Crete (Greece), July 1990.
- 1990 Director, Fibonacci Institute for the Foundations of Computer Science, Trento, Italy.
- 1993 General Chair, IEEE Symposium on Parallel and Distributed Computing, Dallas (Texas),
December 1993.
- 1999 Chair, International Goedel Prize Committee.
- 2000- Member, Review Committee for the Mathematics and Computer Science Division
of Argonne National Laboratory of the University of Chicago.
- 2000-2004 Member, Scientific Committee of Istituto per l’Elaborazione dell’Informazione
(currently: Istituto per la Scienza e la Tecnologia dell’Informazione),
National Research Council, Italy
- 2003-2005 Member, Scientific Advisory Board VICOM Project (Virtual Immersive Communications)
Ministry of Industrial and University Research, Italy.
- 2003- Member, International Advisory Panel, Graduate School for Science and Engineering,
National University of Singapore.
- 2006- Standing Member, Expert Panel for In Information Technology and Mathematics,
Ministry of Education, The Republic of Singapore.

Experience-Editorial

- 1978-1982 Associate Editor (Applied Theory of Computation-Design of Algorithms),
IEEE Transactions on Computers
- 1982-2003 Associate Editor, SIAM Journal on Computing
- 1982-1988 Editor, “Advances in Computing Research,” a research annual published by

JAI Press, Inc., Greenwich, Conn.

- 1985- Editor and Member of Executive Committee, *Algorithmica*
- 1985-2002 Member of Editorial Board, *Discrete and Computational Geometry*
- 1985-1989 Member of Editorial Board, *Journal of Symbolic Computation*
- 1984-1993 Editor, *Information and Computation*
- 1988- Member of Editorial Board, *Theoretical Computer Science*
- 1989-1994 Member of Editorial Board, *Graphical Models and Image Processing*
- 1991- Honorary Editor, *Computational Geometry-Theory and Applications*
- 1991-2005 Member of Editorial Board, *International Journal of Computational Geometry and Applications*.
- 1999-2005 Managing Editor, *Foundations of Computer Science*.

Society Memberships

Institute of Electrical and Electronics Engineers.

Association for Computing Machinery.

International Society of Computational Biology.

Summary of Research History and Outline of Current Interest

Dr. Preparata's initial research interest lay prevalently in switching theory and in coding theory. In switching theory he investigated sequential machines, diagnosable systems and universal modules. In coding theory he developed optimal convolutional codes (known as the Berlekamp-Preparata codes) and optimal nonlinear codes (known as the Preparata codes). Out of his research in optimal boolean networks he developed an interest for sorting networks, and his interest for computer algorithms grew out of such considerations.

Currently, his area of interest is, in its broadest sense, the design and analysis of computer algorithms, with particular emphasis on combinatorial problems, computational geometry, parallel computation, and computational molecular biology.

Books

1. (with R.T. Yeh) *Introduction to Discrete Structures*, Addison-Wesley, Reading, Mass., 1973.
 Italian translation, 1976
 Japanese translation, 1980
 Czech translation, 1982
2. *Introduction to Computer Engineering*, Harper-Row, 1985, John Wiley, 1988.
 Italian translation, 1987
3. (with M.I. Shamos) *Computational Geometry*, Springer-Verlag, 1985.

Russian translation, 1989
Chinese translation, 1990
Japanese translation, 1992
Czech translation, 2003

4. *Lectures on Parallel Computation* (compiled and edited by colleagues at Kyoto University), Kyoritsu (Japan), 1996.

Chapters in Book

“Computational complexity,” in *MAA Studies in Mathematics*, Volume 22: “Studies in Computer Science,” (S.V. Pollock, Editor), 1982.

“Combinational Networks and Switching Algebra,” in *The Electrical Engineering Handbook*, pp. 1695-1711 (R.C. Dorf, Editor; CRC Press) 1993.

”Sequence reconstruction from nucleic acid micro-array data”, (with E. Upfal and S.A.Heath) in *Analytic techniques for DNA sequencing*, B. Nunnally ed., M. Dekker, pp. 177-193, 2005

Books Edited

1. *Theoretical Computer Science*, C.I.M.E. Summer Schol, Bressanone, Italy; Cremonese, Rome, 1975.
2. Proc. 15th Annual Allerton Conference on Communication, Control and Computing, Monticello, Illinois; October 1977.
3. Proc. 17th Annual Allerton Conference on Communication, Control and Computing, Monticello, Illinois; October 1979.
4. *Advances in Computing Research*, Vol. I: Computational Geometry, JAI Press, Greenwich, Conn., 1983.
5. *Advances in Computing Research*, Vol. II: VLSI Theory, JAI Press, Greenwich, Conn., 1984.
6. *Advances in Computing Research*, Vol. IV: Parallel and Distributed Computing, JAI Press, Greenwich, Conn., 1987.

Journal Articles

1. "Probability of Undetected Errors in Punched-Card Read-Checking Electronic Computers," (in Italian), *Schede Perforate e Calcolo Elettronico*, V, March 1962.
2. "Systematic Construction of Optimal Linear Recurrent Codes for Burst Error Correction," *Calcolo*, Vol. 1, No. 2, pp. 147-153, June 1964.
3. "State-Logic Relations for Autonomous Sequential Networks," *IEEE Trans. on Electronic Computers*, Vol. EC-13, No. 5, pp. 542-548, October 1964.
4. "Traffic Analysis of a Buffered Digital Data Acquisition System," *Calcolo*, Vol. 2, No. 1, pp. 113-126, January 1965.
5. "On the Realizability of Special Classes of Autonomous Sequential Networks," *IEEE Trans. on Electronic Computers*, Vol. EC-14, No. 6, pp. 791-797, December 1965.
6. "A Note on Non-Singular Autonomous Sequential Networks and Invertible Boolean Systems," *Ciencias de la Informacion y la Computation* (Mexico), Vol. 1, No. 2, pp. 25-29, Sept.-Dec. 1966.
7. "Convolutional Transformation of Binary Sequences: Boolean Functions and Their Resynchronizing Properties," *IEEE Trans. on Electronic Computers*, Vol. EC-15, No. 6, pp. 898-908, December 1966.
8. With G. Metze and R.T. Chien: "On the Connection Assignment Problem of Diagnosable Systems," *IEEE Trans. on Electronic Computers*, Vol. EC-16, No. 6, pp. 848-854, Dec. 1967.
9. "Weight and Distance Structure of Nordstrom-Robinson Quadratic Code," *Information and Control*, Vol. 12, No. 5/6, pp. 466-473, May-June 1968.
10. "Convolutional Transformation and Recovery of Binary Sequences," *IEEE Trans. on Computers*, Vol. C-17, No. 7, pp. 649-655, July 1968.
11. "A Class of Optimum Nonlinear Double-Error-Correcting Codes," *Information and Control*, Vol. 13, No. 4, pp. 378-401, October 1968.
12. "An Estimate of the Length of Diagnostic Tests," *IEEE Trans. on Reliability*, Vol. 18, No. 3, pp. 131-136, August 1969.
13. With D.E. Muller, "Generation of Near-Optimal Universal Boolean Functions," *Journal of Computer and System Science*, Vol. 4, No. 2, pp. 93-102, April 1970.
14. "A New Look at the Golay (23,12) Binary Code," *IEEE Trans. on Information Theory*, Vol. 16, No. 4, pp. 510-511, July 1970.
15. "On the Design of Universal Boolean Functions," *IEEE Trans. on Computers*, Vol. C-20, No. 4, pp. 418-423, April 1971.
16. With D.E. Muller, "On the Delay Required to Realize Boolean Functions," *IEEE Trans. on Computers*, Vol. C-20, No. 4, pp. 459-461, April 1971.

17. With A. Martelli, "Tolshchina i kaskadnaiya dekompozitsiya perestanovok" (Thickness and cascade decomposition of permutations), *Avtomatika i Telemekhanika*, No. 7, pp. 98-108, July 1971 (in Russian).
18. With R.T. Chien and S.J. Hong, "Some Results in the Theory of Arithmetic Codes," *Information and Control*, Vol. 19, No. 3, pp. 246-263, October 1971.
19. "On the Representation of Integers in Nonadjacent Form," *SIAM Journal of Applied Mathematics*, Vol. 21, No. 4, pp. 630-635, December 1971.
20. With S.R. Ray, "An Approach to Artificial Nonsymbolic Cognition," *Journal of Information Sciences*, Vol. 4, pp. 65-86, Spring 1972.
21. "Analysis of Traffic Flow on a Signalized One-Way Artery," *Transportation Science*, Vol. 6, No. 1, pp. 32-51, February 1972.
22. "Universal Logic Modules of a New Type," *IEEE Transactions on Computers*, Vol. C-21, No. 6, pp. 585-588, June 1972.
23. With R.T. Yeh, "Continuously Valued Logic," *Journal of Computer and System Science*, Vol. 6, No. 5, pp. 397-418, October 1972.
24. "On Multitransmission Networks," *IEEE Transactions on Circuit Theory*, Vol. CT-20, No. 1, pp. 67-69, January 1973.
25. With L. Bellato, "Error Detection and Synchronization with Pseudoternary Codes for Data Transmission," *Alta Frequenza*, Vol. 42, No. 6, pp. 134-139, June 1973.
26. With J. Nievergelt, "Difference-Preserving Codes," *IEEE Trans. on Information Theory*, Vol. IT-20, No. 5, pp. 643-649, September 1974.
27. With D.E. Muller, "Bounds to Complexities of Networks for Sorting and for Switching," *Journal of the ACM*, Vol. 22, No. 2, pp. 195-201, April 1975.
28. With D.E. Muller, "The Time Required to Evaluate Division-Free Arithmetic Expressions," *Information Processing Letters*, Vol. 3, No. 5, pp. 144-146, May 1975.
29. With H.T. Kung and F. Luccio, "On Finding the Maxima of a Set of Vectors," *Journal of the ACM*, Vol. 22, No. 4, pp. 469-476, October 1975.
30. "A Fast Stable Sorting Algorithm with Absolutely Minimum Storage," *Theoretical Computer Science*, Vol. 1, No. 2, pp. 185-190, December 1975.
31. With G. Galbiati, "On Permutation Embedding Sequences," *SIAM Journal on Applied Mathematics*, Vol. 30, No. 3, pp. 421-423, May 1976.
32. With D.E. Muller, "Efficient Parallel Evaluation of Boolean Expressions," *IEEE Transactions on Computers*, Vol. C-25, No. 5, pp. 548-549, May 1976.
33. With D.E. Muller, "Restructuring of Arithmetic Expressions for Parallel Evaluation," *Journal of the ACM*, Vol. 23, No. 3, pp. 534-543, July 1976.
34. With F. Luccio, "Storage for Consecutive Retrieval," *Information Processing Letters*, Vol. 5, No. 3, pp. 78-81, August 1976.

35. With S.J. Hong, "Convex Hulls of Finite Sets in Two and Three Dimensions," *Communications of the ACM*, Vol. 20, No. 2, pp. 87-93, February 1977.
36. With D.E. Muller and A.B. Barak, "Reduction of Depth of Boolean Networks With a Fan-in Constraint," *IEEE Transactions on Computers*, Vol. C-26, No. 5, pp. 474-479, May 1977.
37. With D.V. Sarwate, "Computational Complexity of Fourier Transforms Over Finite Fields," *Mathematics of Computation*, Vol. 31, No. 139, pp. 740-751, July 1977.
38. With D.T. Lee, "Location of a Point in a Planar Subdivision and Its Applications," *SIAM Journal on Computing*, Vol. 6, No. 3, pp. 594-606, September 1977.
39. With D.S. Johnson, "The Densest Hemisphere Problem," *Theoretical Computer Science*, Vol. 6, pp. 93-107, January 1978.
40. With V.A. DiEuliis, "Spectrum Shaping With Codes With Finite Autocorrelation Sequence," *IEEE Transactions on Communications* (Concise paper), Vol. 26, No. 4, pp. 474-478, April 1978.
41. With D.V. Sarwate, "An Improved Parallel Processor Bound in Fast Matrix Inversion," *Information Processing Letters*, Vol. 7, No. 3, pp. 148-150, April 1978.
42. "New Parallel Sorting Schemes", *IEEE Transactions on Computers*, Vol. C-27, No. 7, pp. 669-673, July 1978.
43. With D.E. Muller, "Finding the Intersection of Two Convex Polyhedra," *Theoretical Computer Science*, vol. 7, No. 2, pp. 217-236, October 1978.
44. D.T. Lee, "The All-Nearest Neighbor Problem for Convex Polygons," *Information Processing Letters*, Vol. 7, No. 4, pp. 189-192, June 1978.
45. With M.R. Garey, D.S. Johnson, and R.E. Tarjan, "Triangulating a Simple Polygon," *Information Processing Letters*, Vol. 7, No. 4, pp. 175-179, June 1978.
46. With D.E. Muller, "Finding the Intersection of n Half-Spaces in Time $O(n \log n)$," *Theoretical Computer Science*, Vol. 8, No. 7, pp. 45-55, January 1979.
47. With L. Adleman, K.S. Booth, and W.L. Ruzzo, "Improved Time and Space Bounds for Boolean Matrix Multiplication," *Acta Informatica*, Vol. 11, pp. 61-70, 1978.
48. With D.T. Lee, "An Optimal Algorithm for Finding the Kernel of a Polygon," *Journal of the ACM*, Vol. 26, No. 3, pp. 415-421, July 1979.
49. "An Optimal Real-Time Algorithm for Planar Convex Hulls," *Communications of the ACM*, Vol. 27, No. 7, pp. 402-405, July 1979.
50. "A Note on the Location of a Set of Points in a Planar Subdivision," *SIAM Journal on Computing*, Vol. 8, No. 4, pp. 542-545, November 1979.
51. With W. Lipski, Jr., "Finding the Contour of a Union of Iso-Oriented Rectangles," *Journal of Algorithms*, Vol. 1, pp. 235-246, 1980.
52. With J. Vuillemin, "Area-Time Optimal VLSI Networks for Multiplying Matrices," *Information Processing Letters*, Vol. 11, No. 2, pp. 77-80, October 1980.

53. With W. Lipski, Jr., "Segments, Rectangles, Contours," *Journal of Algorithms*, Vol. 2, pp. 63-76, 1981.
54. With J. Vuillemin, "The Cube-Connected-Cycles: A Versatile Network for Parallel Computation," *Communications of the ACM*, Vol. 24, No. 5, pp. 300-309, May 1981.
55. "A New Approach to Planar Point Location," *SIAM Journal on Computing*, Vol. 10, No. 3, pp. 473-482, August 1981.
56. With W. Lipski, Jr., "Efficient Algorithms for Finding Maximum Matchings in Convex Bipartite Graphs and Related Problems," *Acta Informatica*, Vol. 15, pp. 329-346, 1981.
57. With K.J. Supowit, "Testing a Simple Polygon for Monotonicity," *Information Processing Letters*, Vol. 12, No. 4, pp. 161-164, August 1981.
58. With J.L. Bentley and M.G. Faust, "Approximation Algorithms for Convex Hulls," *Communications of the ACM*, Vol. 25, No. 1, pp. 64-68, January 1982.
59. With J. Nievergelt, "Plane-Sweep Algorithms for Intersecting Geometric Figures," *Communications of the ACM*, Vol. 25, No. 10, pp. 739-747, October 1982.
60. With D.T. Lee, "An Improved Algorithm for Rectangle Containment," *Journal of Algorithms*, Vol. 3, pp. 213-224, 1982.
61. With G. Bilardi and M. Pracchi, "A Critique of Network Speed in VLSI Models of Computation," *IEEE Journal of Solid State Circuits*, Vol. SC-17, No. 4, pp. 696-702, August 1982.
62. With H. Edelsbrunner, H.A. Maurer, A.L. Rosenberg, E. Welzl, and D. Wood, "Stabbing Line Segments," *BIT*, Vol. 22, pp. 274-281, 1982.
63. "An Area-Time Optimal Mesh-Connected Integer Multiplier," *IEEE Transactions on Computers*, Vol. C-32, No. 2, pp. 194-198, February 1983.
64. With A. Apostolico, "Optimal Off-Line Detection of Repetitions in a String," *Theoretical Computer Science*, Vol. 22, pp. 297-315, 1983.
65. "Optimal Three-Dimensional VLSI Layouts," *Mathematical System Theory*, Vol. 16, pp. 1-8, 1983.
66. With G.M. Baudet and J. Vuillemin, "Area-Time Optimal VLSI Circuits for Convolution," *IEEE Transactions on Computers*, Vol. C-32, No. 7, pp. 684-688, July 1983.
67. With K. Mehlhorn, "Area-Time Optimal VLSI Integer Multiplier With Minimum Computation Time," *Information and Control*, Vol. 58, No. 1-3, pp. 137-156, 1983.
68. With W. Lipski, Jr., "Optimal Three-Layer Channel Routing," *IEEE Transactions on Computers*, Vol. C-33, No. 5, pp. 427-437, May 1984.
69. With G. Bilardi, "An Architecture for Bitonic Sorting with Optimal VLSI Performance," *IEEE Transactions on Computers*, Vol. C-33, No. 7, pp. 646-651, July 1984.
70. With D.T. Lee, "Euclidean Shortest Paths in the Presence of Rectilinear Barriers," *Networks*, Vol. 14, pp. 393-410, 1984.

71. With D.T. Lee, "Computational Geometry: A Survey," (Invited paper), *IEEE Transactions on Computers*, Vol. C-33, No. 12, pp. 1072-1101, December 1984.
72. With G. Bilardi, "On the VLSI Optimality of the AKS Network," *Information Processing Letters*, Vol. 20, pp. 55-59, February 1985.
73. With G. Bilardi, "A Minimum Area VLSI Network for $O(\log n)$ time sorting," *IEEE Transactions on Computers*, Vol. C-34, No. 4, pp. 336-343, April 1985.
74. With M. Sarrafzadeh, "Compact Channel Routing of Multiterminal Nets," *Annals of Discrete Mathematics*, Vol. 25, pp. 255-280, 1985.
75. With A. Apostolico, "Structural Properties of the String Statistics Problem," *Journal of Computer and System Sciences*, Vol. 31, No. 3, pp. 394-411, December 1985.
76. With K. Mehlhorn, "Routing Through a Rectangle," *Jour. Assoc. Comp. Mach.*, Vol. 33, No. 1, pp. 60-85, January 1986.
77. With B. Chazelle, "Half Space Range Search: An Algorithmic Application of k -sets," *Discrete and Computational Geometry*, Vol. 1, No. 1, pp. 83-94, 1986.
78. With G. Bilardi, "Area-time Lower-bound Techniques with Applications to Sorting," *Algorithmica*, Vol. 1, No. 1, pp. 65-91, January 1986.
79. With B. Chazelle, R. Cole, and C. Yap, "New Upper Bounds for Neighbor Searching," *Information and Control*, Vol. 68, No. 1-3, pp. 105-124, January 1986.
80. With K. Mehlhorn and M. Sarrafzadeh, "Channel Routing in Knock-Knee Mode: Simplified Algorithms and Proofs," *Algorithmica*, Vol. 1, No. 2, pp. 213-221, 1986.
81. With W. Lipski, Jr., "A Unified Approach to Layout Wirability," *Mathematical System Theory*, Vol. 19, pp. 189-203, 1987.
82. With K. Mehlhorn, "Area-Time Optimal Division for $T = O(\log n)^{1+\epsilon}$," *Information and Control*, Vol. 72, No. 3, pp. 270-282, March 1987.
83. With H. Alt, T. Hagerup, K. Mehlhorn, "Deterministic Simulation of Idealized Parallel Computers on More Realistic Ones," *SIAM Journal on Computing*, Vol. 16, No. 5, pp. 808-835, October 1987.
84. With M. Sarrafzadeh, "A Bottom-up Layout Technique Based on Two Rectangle Routing," *Integration*, Vol. 5, pp. 231-246, 1987.
85. With H. Edelsbrunner, "Minimum Polygonal Separation," *Information and Computation*, Vol. 77, No. 3, pp. 218-232, June 1988.
86. With R.M. Preparata, E.B. Meyer, E.M. Simon, C.R. Vossbrinck, and D.L. Nanney, "Ciliate evolution: The Ribosomal Phylogeny of Tetrahymenine Ciliates," *Jour. Molecular Evolution*, vo.. 28, pp. 427-442, 1989.
87. With D.L. Nanney, R.M. Preparata, E.B. Meyer, and E.M. Simon, "Shifting Ditypic Site Analysis: Heuristics for Extending the Phylogenetic Range of Nucleotide Sequences in Sankoff String Analysis," *Jour. Molecular Evolution*, Vo.. 28, pp. 451-459, 1989.

88. With G. Bilardi, "Size-time Complexity of Boolean Networks for Prefix Computations," *Journal of the ACM*, Vol. 36, No. 2, pp. 362-382, April 1989.
89. With R. Tamassia, "Fully Dynamic Point Location in Monotone Subdivisions," *SIAM Journal on Computing*, Vol. 18, No. 4, pp. 811-830, August 1989.
90. "Holographic Dispersal and Recovery of Information," *IEEE Transactions on Information Theory*, Vol. 35, No. 5, pp. 1123-1124, September 1989.
91. With D.T. Lee, "Parallel Batched Planar Point Location on the CCC," *Information Processing Letters*, Vol. 33, pp. 175-179, December 1989.
92. "Planar Point Location Revisited," *International Journal of Foundations of Computer Science*, Vol. 1, No. 1, pp. 71-86, March 1990.
93. With G. Bilardi, "Characterization of Associative Operations with Prefix Circuits of Constant Depth and Linear Size," *SIAM Journal on Computing*, Vol. 19, no. 2, pp. 246-255, April 1990.
94. With J. Vuillemin, "Practical Cellular Dividers," *IEEE Trans. on Computers*, Vol. 39, No. 5, pp. 605-614, May 1990.
95. With R. Tamassia, "Dynamic Maintenance of Planar Digraphs, with Applications," *Algorithmica*, Vol. 5, pp. 509-528, 1990.
96. With J.S. Vitter and M. Yvinec, "Computation of the Axial View of a Set of Isothetic Parallelepipeds," *ACM Trans. on Computer Graphics*, Vol. 9, No. 5, pp. 278-300, July 1990.
97. With P. Alevizos and J.D. Boissonnat, "An Optimal Algorithm for the Boundary of a Cell in a Union of Rays," *Algorithmica*, Vol.5, pp. 573-590, 1990.
98. With R. Tamassia, "Dynamic Planar Point Location with Optimal Query Time," *Theoretical Computer Science*, Vol. 74, pp. 95-114, 1990.
99. With H. Edelsbrunner and D.B. West, "Tetrahedrizing Point Sets in Three Dimensions," *Journal of Symbolic Computation*, Vol. 10, pp. 335-347, 1990.
100. With S.W. Hornick, "Deterministic P-RAM Simulation with Constant Redundancy," *Information and Computation*, Vol. 92, No. 1, pp. 81-95, May 1991.
101. "Inverting a Vandermonde Matrix in Minimum Parallel Time," *Information Processing Letters*, Vol. 38, pp. 291-294, June 1991.
102. With J.D. Boissonnat and O. Devillers, "Computing the Union of 3-Colored Triangles," *International Journal of Computational Geometry and Applications*, Vol. 1, No. 2, pp. 187-198, June 1991.
103. With D. Zhou and S.M. Kang, "Interconnection Delay in Very High-Speed VLSI," *IEEE Trans. on Circuits and Systems*, Vol. 28, No. 7, pp. 779-790, July 1991.
104. With D.E. Muller, "Parallel Restructuring and Evaluation of Expressions," *Journal of Computer and System Sciences*, Vol. 44, No. 1, pp. 43-62, February 1992.

105. With J.S. Vitter and M. Yvinec, "Output-Sensitive Generation of the Perspective View of Isothetic Parallepipeds," *Algorithmica*, Vol. 8, pp. 257-283, 1992.
106. With R. Tamassia, "Efficient Point Location in a Convex Spatial Cell Complex," *SIAM Journal on Computing*, Vol. 21, No. 2, 267-280, April 1992.
107. With N. Amato, "The Parallel 3D Convex Hull Problem Revisited," *International Journal of Computational Geometry and Applications*, Vol. 2, No. 2, 163-173, 1992.
108. With G. Bilardi, "Memory Requirements of First-Order Digital Filters," *IEEE Trans. on Circuits and Systems, II*, Vol. 36, No. 6, pp. 348-355, June 1992.
109. With J.S. Vitter, "A Simplified Technique for Hidden-Line Elimination in Terrains," *International Journal of Computational Geometry and Applications*, Vol. 3, No. 2, pp. 167-181, 1993.
110. With R. Janardan, "Widest Corridor Problems," *Nordic Journal of Computing*, pp. 231-245, 1994.
111. With J.B. Boissonnat, O. Devillers, and L. Donati, "Motion Planning of Legged Robots: The Spider Robot Problem," *International Journal of Computational Geometry and Applications*, Vol. 5, n. 1-2, pp. 3-20 (1995).
112. With G. Bilardi, "Horizons of Parallel Computation," *Journal of Parallel and Distributed Computing*, Vol. 27, pp. 172-182 (1995).
113. With V. Pan, "Work-Preserving Acceleration of Parallel Matrix Computations," *SIAM Journal on Computing*, Vol. 24, n. 4, pp. 811-821 (1995).
114. With N. Amato, "A Time-Optimal Parallel Algorithm for 3D Convex Hulls," *Algorithmica*, Vol. 14, n. 2, pp. 169-182 (1995).
115. With Y.-J. Chiang and R. Tamassia, "A Unified Approach to Dynamic Point Location, Ray Shooting, and Shortest Paths in Planar Maps," *SIAM Journal on Computing*, Vol. 25, No. 1, pp. 207-233 (1996).
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