Curriculum Vitae

1. **R. Iris Bahar**
   Professor of Engineering
   Professor of Computer Science
   School of Engineering

2. **Education:**

   Ph.D., Electrical Engineering
   University of Colorado, Boulder, December 1995
   Dissertation: Methods for Timing Analysis and Logic Synthesis to Decrease Power Dissipation

   M.S., Electrical Engineering
   University of Illinois, Urbana, May 1987

   B.S., Computer Engineering
   University of Illinois, Urbana, January 1986

3. **Professional Appointments:**

2012–present	**Professor**, School of Engineering, Brown University. Member of the Electrical Sciences and Computer Engineering Group and the Laboratory for Engineering Man/Machine Systems (LEMS). Research interests low-power and fault-tolerant design, VLSI chip design, computer architecture and nanosystem design.
2003–2012	**Associate Professor**, Division of Engineering, Brown University. Member of the Electrical Sciences and Computer Engineering Group and the Laboratory for Engineering Man/Machine Systems (LEMS).
2007–2008	**Visiting Professor**, Department of Automation and Information, Politecnico di Torino, Italy. Working with researchers on power and thermal issues in computer system design.
2000–2001	**Visiting Researcher**, Compaq Corporation, Shrewsbury, MA. Worked with researcher in microprocessor design group on low-power multithreaded architecture designs.
1996–2003	**Assistant Professor**, Division of Engineering, Brown University. Member of the Laboratory for Engineering Man/Machine Systems (LEMS). Research interests in CAD for low power VLSI chip design.

4. **Completed Research and Scholarship Work:**

   a. **Books and Book Chapters**

   [1] M. B. Tahoori, N. K. Jha, R. I. Bahar, "Testing Aspects of Nanotechnology Trends," Chapter 17 in *Systems on Chip Test Architectures: Nanometer Design for Testability*, L. T. Wang, C. Stroud, and N. Touba, editors, Elsevier Publishers (Morgan Kaufmann), 2008, ISBN: 978-0-12-373973-5.

   [2] K. Nepal, R. I. Bahar, R. I. Bahar, J. Mundy, W. Patterson, A. Zaslavsky, "Designing Nanoscale Logic Circuits Based on Principles of Markov Random Fields," Chapter

12 in *Emerging Nanotechnologies: Test, Defect Tolerance and Reliability*, M. Tehranipoor, editor, Springer Publishers, 2008, ISBN: 978-0-387-74746-0.

[3] R. I. Bahar, J. Chen, J. Mundy, "A Probabilistic-Based Design for Nanoscale Computation," Chapter 5 in, *Nano, Quantum and Molecular Computing: Implications to High Level Design and Validation*, Springer, 2004, ISBN: 978-1-4020-8067-8.

[4] S. Shukla and R. I. Bahar, editors, *Nano, Quantum and Molecular Computing: Implications to High Level Design and Validation*, Springer, 2004, ISBN: 978-1-4020-8067-8.

b. Refereed Journal Articles

[5] Dimitra Papagiannopoulou, Tali Moreshet, Andrea Marongiu, Luca Benini, Maurice Herlihy, R. Iris Bahar, "Hardware Transactional Memory Exploration in Coherence-free Many-core Architectures," *International Journal of Parallel Programming (Springer)*. April 2018. DOI 10.1007/s10766-018-0569-7.

[6] C. Harris, R. I. Bahar, "Towards the Simulation Based Design and Validation of Mobile Robotic Cyber-physical Systems," *Journal of Low Power Electronics (JOLPE)*. Vol. 14, No. 1, March 2018, pp. 148-156. American Scientific Publishers. DOI 10.1166/jolpe.2018.1540

[7] Dimitra Papagiannopoulou, Andrea Marongiu, Tali Moreshet, Maurice Herlihy, R. Iris Bahar, "Edge-TM: Exploiting Transactional Memory for Error Tolerance and Energy Efficiency," *ACM Transactions on Embedded Computing Systems (TECS)*. Vol. 16, Issue 5s, Article 153. Also appearing as regular presentation at the *IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES)*, October, 2017. DOI 10.1145/3126556

[8] M. Donato, R. Iris Bahar, W. Patterson, A. Zaslavsky, "A Subthreshold Noise Transient Simulator Based on Integrated Random Telegraph and Thermal Noise Modeling," *IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD)*. Vol. 37, Issue 3, pp. 643-656. March, 2018. DOI 10.1109/TCAD.2017.2717705

[9] Kumud Nepal, Soheil Hashemi, Hokchhay Tann, R. Iris Bahar, Sherief Reda, "Automated High-Level Generation of Low-Power Approximate Computing Circuits," *IEEE Transactions on Emerging Topics in Computing (TETC)*, Aug. 2016. DOI 10.1109/TETC.2016.2598283.

[10] Kundan Nepal, Soha Alhelaly, Jennifer Dworak, R. Iris Bahar, Theodore Manikas, Ping Gui, "Repairing a 3D Die-Stack Using Available Programmable Logic," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*. Vol 34, No. 5, May 2015, pp. 849-861. DOI 10.1109/TCAD.2015.2399441.

[11] D. Papagiannopoulou, G. Capodanno, T. Moreshet, M. Herlihy, R. I. Bahar, "Energy-Efficient and High-Performance Lock Speculation Hardware for Embedded Multicore Systems," *ACM Transactions on Embedded Computing Systems (TECS)*. Vol. 14, Issue 3, Article 51, May 2015. DOI: http://dx.doi.org/10.1145/2700097

[12] O. Ulusel, K. Nepal, R. I. Bahar, S. Reda, "Fast Design Exploration for Performance, Power and Accuracy Tradeoffs in FPGA-based Accelerators," *ACM Transactions on Reconfigurable Technology and Systems*. 7, 1, Article 4. (February 2014), 22 pages. DOI=10.1145/2567661 http://dx.doi.org/10.1145/2567661.

[13] J. Dworak, Kundan Nepal, N. Alves, Y. Shi, N. Imbriglia, R. I. Bahar, "Using Implications to Choose Tests Through Suspect Fault Identification" *ACM Journal on Design Automation of Electronic Systems (TODAES)*, Vol. 18, Issue 1, January 2013, pp. 14:1-14:19. DOI 10.1145/2390191.2390205

[14] C. Ferri, D. Papagiannopoulou, A. Calimera, R. I. Bahar, "NBTI-Aware Data Allocation Strategies for Scratchpad Based Embedded Systems," *Springer Journal of Electronic Testing: Theory and Applications (JETTA)*, Vol. 28, No. 3, May/June 2012, pp. 349-363. DOI 10.1007/s10836-012-5295-2

[15] P. Jannaty, F. C. Sabou, Son T. Le, M. Donato, R. I. Bahar, W. Patterson, J. Mundy, A. Zaslavsky, "Shot-Noise-Induced Failure in Nanoscale Flip-Flops—Part I: Numerical Framework," *IEEE Transactions on Electron Devices*, Vol. 59, No. 3, March 2012, pp. 800-806.

[16] P. Jannaty, F. C. Sabou, Son T. Le, M. Donato, R. I. Bahar, W. Patterson, J. Mundy, A. Zaslavsky, "Shot-Noise-Induced Failure in Nanoscale Flip-Flops—Part II: Failure Rates in 10nm Ultimate CMOS," *IEEE Transactions on Electron Devices.* Vol. 59, No. 3, March 2012, pp. 807-812.

[17] D. Tadesse, R. I. Bahar, and J. Grodstein, "Test Vector Generation for Post-Silicon Delay Testing using SAT-Based Decision Problems," *Springer Journal of Electronic Testing: Theory and Applications (JETTA).* Vol. 27, No. 2, May 2011, pp. 123-136. DOI link: 10.1007/s10836-011-5205-z

[18] P. Jannaty, F. C. Sabou, R. I. Bahar, J. Mundy, W. Patterson, A. Zaslavsky, "Full Two-Dimensional Markov Chain Analysis of Thermal Soft Errors in Subthreshold Nanoscale CMOS Devices," *IEEE Transactions on Device and Materials Reliability,* Vol. 11, No. 1, March 2011, pp. 50-59. DOI link: 10.1109/TDMR.2010.2069100

[19] P. Jannaty, F. C. Sabou, M. Gadlage, R. I. Bahar, J. Mundy, W. R. Patterson, R. A. Reed, R. A.Weller, R. D. Schrimpf, A. Zaslavsky, "Two-Dimensional Markov Chain Analysis of Radiation-Induced Soft Errors in Subthreshold Nanoscale CMOS Devices," *IEEE Transactions on Nuclear Science.* Vol. 57, No. 6, December 2010, pp. 3768-3774.

[20] C. Ferri, S. Wood, T. Moreshet, R. I. Bahar, and M. Herlihy, "Embedded-TM: Energy and Complexity-Effective Hardware Transactional Memory for Embedded Multicore Systems," *Elsevier Journal of Parallel and Distributed Computing*. Vol. 70, No. 10, October 2010. DOI link: doi:10.1016/j.jpdc.2010.02.003

[21] N. Alves, A. Buben, K. Nepal, J. Dworak, R. I. Bahar, "A Cost-Effective Approach for Online Error Detection using Invariant Relationships," *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, Vol. 29, No. 5, May 2010, pp. 788-801.

[22] A. Calimera, R. I. Bahar, E. Macii, M. Poncino, "Temperature-Insensitive Dual-Vth Synthesis for Nanometer CMOS Technologies under Inverted Temperature Dependence," *IEEE Transactions on VLSI Systems.* Vol. 18, No. 11, November 2010, pp. 1608-1620.

[23] A. Calimera, R. I. Bahar, E. Macii, M. Poncino, "Dual-Vt Assignment Policies in ITD-Aware Synthesis," *Microelectronics Journal*, Elsevier Publishers. Vol. 41, No. 9, September, 2010.

[24] F. C. Sabou, D. Kazazis, R. I. Bahar, J. Mundy, W. Patterson, A. Zaslavsky, "Markov Chain Analysis of Thermally Induced Soft Errors in Subthreshold Nanoscale CMOS Circuits," *IEEE Transactions on Device and Materials Reliability,* Vol. 9, No. 3, Sept. 2009, pp. 494 – 504.

[25] C. Ferri, S. Reda, and R. I. Bahar, "Parametric Yield Management for 3D ICs: Models and Strategies for Improvement," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Vol. 4, No. 4, October 2008, pp. 19:1-22.

[26] K. Nepal, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Designing Nanoscale Logic Circuits based on Markov Random Fields," *Springer Journal of Electronic Testing: Theory and Applications*, Vol. 23, No. 2, March 22, 2007, pp. 255-266.

[27] C. Ferri, T. Moreshet, R. I. Bahar, L. Benini, and M. Herlihy. "A Hardware/Software Framework for Supporting Transactional Memory in an MPSoC Environment," *SIGARCH Computer Architecture News* Vol. 35, No. 1, March 2007, pp. 47-54.
[28] R. I. Bahar, J. Harlow, D. Hammerstrom, W. H. Joyner Jr., C. Lau, D. Marculescu, A. Orailoglu, M. Pedram, "Architectures for Silicon Nanotechnology and Beyond," *IEEE Computer*, Vol. 40, No. 1, January 2007, pp. 25-33.
[29] K. Nepal, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "The MRF Reinforcer: A Probabilistic Element for Space Redundancy in Nanoscale Circuits," *IEEE MICRO*, Vol. 26, No. 5, September/October 2006, pp. 19–27.
[30] H.Y. Song, K. Nepal, R. I. Bahar, J. Grodstein, "Timing Analysis for Full-Custom Circuits Using Symbolic DC Formulations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, Vol. 25, No. 9, September 2006, pp.1815–1830.
[31] R. I. Bahar, H. Y. Song, K. Nepal, J. Grodstein, "Symbolic Failure Analysis of Complex CMOS Circuits due to Excessive Leakage Current and Charge Sharing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, Vol. 24, No. 5, April 2005, pp. 502-515.
[32] T. Moreshet and R. I. Bahar, "Effects of Speculation on Performance and Issue Queue Design," *IEEE Transaction on VLSI*, Vol. 12, No. 10, October 2004, pp. 1123–1125. Transaction brief.
[33] Y. Bai and R. I. Bahar, "A Low Power In-Order/Out-of-Order Issue Queue," *ACM Transactions on Architecture and Code Optimization*, Vol. 1, No. 2, June 2004, pp. 152-179.
[34] R. I. Bahar, E. T. Lampe, E. Macii, "Power Optimization of Technology-Dependent Circuits Based on Symbolic Computation of Logic Implications," *ACM Transactions on Design Automation of Electronic Systems*. July 2000, pp. 267–293.
[35] R. I. Bahar, H. Cho, G. D. Hachtel, E. Macii, F. Somenzi, "Symbolic Timing Analysis and Re-Synthesis for Low Power of Combinational Circuits Containing False Paths," *IEEE Journal of Computer-Aided Design*, Vol. 16, No. 10, October 1997, pp. 1101-1115.
[36] R. I. Bahar, E. A. Frohm, C. M. Gaona, G. D. Hachtel, E. Macii, A. Pardo, F. Somenzi, "Algebraic Decision Diagrams and their Applications," *Springer Journal of Formal Methods in Systems Design*. Vol. 10, No. 2/3, April 1997, pp. 171-206.
[37] R. Badeau, *et al.*, "A 100-MHz Macropipelined VAX Microprocessor," *IEEE Journal of Solid-State Circuits, Vol. 27, No. 11*, November 1992, pp. 1585-1598.

d. Invited Articles

[38] Y. Liu, Z. Sui, A. Costantini, Z. Ye, S. Lu, O. C. Jenkins, R. I. Bahar, "Robust Object Estimation using Generative-Discriminative Inference for Secure Robotics Applications," *International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, November 2018. Invited paper.
[39] Christopher Harris, R. Iris Bahar, "A Research Tool for the Power and Perforamnce Analysis of Sensor Based Mobile Robots," *New Generation of Circuits and Systems Conference (NGCAS)*, Genova, Italy, September 2017. Invited paper. DOI 10.1109/NGCAS.2017.25
[40] R. Iris Bahar, Alex K. Jones, Srinivas Katkoori, Patrick H. Madden, Diana Marculescu, and Igor L. Markov, "Workshops on Extreme Scale Design Automation (ESDA) Challenges and Opportunities for 2025 and Beyond," *Computing Community Consortium (CCC) Catalyst,* November 2014. Final Report. http://cra.org/ccc/wp-content/uploads/sites/2/2015/05/CCC_ESDA-Report.pdf

[41] R. Iris Bahar, Alex K. Jones, Srinivas Katkoori, Patrick H. Madden, Diana Marculescu, and Igor L. Markov, "'Scaling' the Impact of EDA Education: Preliminary Findings from the CCC Workshop Series on Extreme Scale Design Automation," *IEEE International Conference on Microelectronic Systems Education*. Austin, TX, June 2013. Invited paper.

[42] R. I. Bahar, "Trends and Future Directions in Nano Structure Based Computing and Fabrication," *IEEE/ACM International Conference on Computer Design*, San Jose, CA, October 2006, pp. 522-527. Invited paper.

[43] R. I. Bahar, "Nanoscale Circuits and Architectures for Probabilistic Computation in the Presence of Noise," *Foundations of Nanoscience Conference (FNANO)*, Snowbird, UT, April 2006. Invited paper.

[44] R. I. Bahar, D. Grunwald, B. Calder, "A Comparison of Software Code Reordering and Victim Buffers," *ACM SIGARCH Computer Architecture News*, March 1999.

c. Refereed Articles in Conferences (presenter indicated with *)
(Note that these are high profile conferences with acceptance rates generally less than 30%. Their impact can be as high as the top journals in this research area.)

[45] S. Whang*, T. Rachford, D. Papagiannopoulou, T. Moreshet, R. I. Bahar, "Evaluating Critical Bits in Arithmetic Operations due to Timing Violations," *IEEE High Performance Extreme Computing Conference (HPEC).* September 2017. 10.1109/HPEC.2017.8091090

[46] Christopher Picardo*, Justin Delva, R. Iris Bahar, "Comprehensive Comparison of Gradient-Based Cross-Spectral Stereo Matching Generated Disparity Maps," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS).* August 2017.

[47] T. Carle*, D. Papagiannopoulou, T. Moreshet, A. Marongiu, M. Herlihy, R. I. Bahar, "Thrifty-malloc : un gestionnaire dynamique de mémoire pour systèmes embarqués multicoeurs avec mémoire transactionnelle matérielle," Compas'2017. June 2017

[48] H. Tann*, S. Hashemi, R. I. Bahar, S. Reda, "Hardware-Software Co-design of Highly Accurate Multiplier-free Deep Neural Networks," *IEEE/ACM Design Automation Conference (DAC)*. June 2017.

[49] Soheil Hashemi, Nicholas Anthony, Hokchhay Tann, R. Iris Bahar, Sherief Reda*, "Understanding the Impact of Precision Quantization on the Accuracy and Energy of Neural Networks," *ACM/IEEE Design Automation and Test Conference (DATE)*. March 2017.

[50] Thomas Carle*, Dimitra Papagiannopoulou, Tali Moreshet, Andrea Marongiu, Maurice Herlihy, R. Iris Bahar, "A Resource-Conscious Dynamic Memory Manager for Embedded Multicore Systems," *IEEE/ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, October, 2016.

[51] Hokchhay Tann*, Soheil Hashemi, R. Iris Bahar, Sherief Reda, "Runtime Configurable Deep Neural Networks for Energy-Accuracy Trade-off," *IEEE/ACM International Conference on Hardware/Software Codesign and system Synthesis (CODES),* October 2016.

[52] Onur Ulusel, Christopher Picardo, Christoper Harris, Sherief Reda, R. Iris Bahar*, "Hardware Acceleration of Feature Detection and Description Algorithms on Low-Power Embedded Platforms," *IEEE International Conference on Field-Programmable Logic and Applications (FPL)*, Aug./Sept., 2016.

[53] Marco Donato*, Alexander Zaslavsky, William R. Patterson, R. Iris Bahar, "A Fast Simulator for the Analysis of Sub-Threshold Thermal Noise Transients," *IEEE/ACM Design Automation Conference (DAC)*, June 2016.

[54] Soheil Hashemi*, R. Iris Bahar, Sherief Reda, "A Methodology for Design of Low-Power Scalable Approximate Integer Dividers," *IEEE/ACM Design Automation Conference (DAC)*, June 2016.

[55] Xijing Han*, Marco Donato, R. Iris Bahar, Alexander Zaslavsky, William R. Patterson, "Design of Error-resilient Logic Gates with Reinforcement Using Implications," *ACM Great Lakes Symposium on VLSI Design (GLSVLSI)*, May 2016.

[56] Soheil Hashemi*, R. Iris Bahar, Sherief Reda, "DRUM: A Dynamic Range Unbiased Multiplier for Approximate Applications," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2015. **Best paper nomination.**

[57] Marco Donato*, R. Iris Bahar, William Patterson and Alexander Zaslavsky, "A Simulation Framework for Analyzing Transient Effects Due to Thermal Noise in Sub-Threshold Circuits," *ACM Great Lakes Symposium on VLSI Design (GLSVLSI)*, May 2015. DOIlink: 10.1145/2742060.2742066

[58] Dimitra Papagiannopoulou*, Andrea Marongiu, Tali Moreshet, Maurice Herlihy, Luca Benini, R. Iris Bahar, "Playing with Fire: Transactional Memory Revisited for Error-Resilient and Energy-Efficient MPSoC Execution," *ACM Great Lakes Symposium on VLSI Design (GLSVLSI)*, May 2015. DOIlink: 10.1145/2742060.2742090

[59] Dimitra Papagiannopouou*, Tali Moreshet, R. Iris Bahar, Andrea Morongiou, Luca Benini, Maurice Herlihy, "Speculative Synchronization for Coherence-free Embedded NUMA Architectures," *International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, July 2014. DOI link: 10.1109/SAMOS.2014.6893200. **Best paper award**.

[60] Kumud Nepal*, Yueting Li, R. Iris Bahar, and Sherief Reda, "ABACUS: A Technique for Automated Behavioral Synthesis for Approximate Computing Circuits," submitted to the *ACM/IEEE Design Automation and Test Conference (DATE)*. March 2014. Acceptance rate for regular papers is 23%. DOI link: 10.7873/DATE.2014.374

[61] Kundan Nepal*, X. Shen, J. Dworak, T. Manikas, R. I. Bahar, "Harnessing an FPGA for Built-in Self-Repair in a 3D Die Stack," *IEEE International Symposium on Defect and Fault Tolerance*, October 2013. Poster Presentation.

[62] Papagiannopoulou*, P. Prasertsom and R. I. Bahar, "Flexible Data Allocation for Scratch-pad Memories to Reduce NBTI Effects", *IEEE International Symposium on Quality Electronic Design*, March 2013.

[63] R. Le*, J. L. Mundy, R. I. Bahar, "High Perfomance Parallel JPEG2000 Streaming Decoder Using GPGPU-CPU Heterogeneous System," *IEEE International Conference on Application-specific Systems, Architectures and Processors,* July 2012. Regular paper. Acceptance rate for regular papers 35%.

[64] M. Donato*, F. Cremona, W. Jin, R. I. Bahar, W. Patterson, A. Zaslavsky, J. Mundy, "A Noise-Immune Sub-Threshold Circuit Design Based on Selective use of Schmitt-Trigger Logic," *ACM Great Lakes Symposium on VLSI*, May 2012, pp. 39-44. DOI link: 10.1145/2206781.2206792. Regular paper. Acceptance rate for regular papers 20%.

[65] Kumud Nepal*, O. Ulusel*, R. I. Bahar, S. Reda, "Fast Multi-Objective Algorithmic-Design Co-Exploration for FPGA-based Accelerators," *20th Annual International*

IEEE Symposium on Field-Programmable Custom Computing Machines, April 29-May 1, 2012. Poster presentation.

[66] C. Ferri, A. Marongiu, B. Lipton*, R. I. Bahar, T. Moreshet, L. Benini, "SoC-TM: Integrated HW/SW Support for Transactional Memory Programming on Embedded MPSoCs," *IEEE International Conference on Hardware/Software Co-Design and System Synthesis*, October, 2011, pp. 39-48. **Best Paper Nominee**. Acceptance rate 25%.

[67] R. Le*, J. Mundy, R. I. Bahar, "A Novel Parallel Tier-1 Coder for JPEG2000 using GPUs," *IEEE Symposium on Application Specific Processors (SASP)*, June, 2011, pp. 129-136. DOI link: 10.1109/SASP.2011.5941091. Acceptance rate for full papers 29%.

[68] C. Ferri*, D. Papagiannopoulou, A. Calimera, R. I. Bahar, "NBTI-Aware Data Allocation Strategies for Scratchpad Based Embedded Systems," *IEEE Latin American Test Workshop*, March 2011, pp. 1-6. DOI link: 10.1109/LATW.2011.5985932. Invited paper.

[69] N. Alves, Y. Shi*, K. Nepal, J. Dworak, R. I. Bahar, "Enhancing Online Error Detection through Area-Efficient Multi-Site Implications," *IEEE VLSI Test Symposium*, May, 2011, pp. 241-246. DOI link: 10.1109/VTS.2011.5783728.

[70] N. Alves*, K. Nepal, J. Dworak, R. I. Bahar, "Improving the Testability and Reliability of Sequential Circuits with Invariant Logic," *ACM Great Lakes Symposium on VLSI*, May 2010, pp. 131-134. Poster presentation. DOI link: 10.1145/1785481.1785513. Overall acceptance rate 50%.

[71] P. Jannaty*, F. C. Sabou, D. Kazazis, R. I. Bahar, J. Mundy, W. Patterson, A. Zaslavsky, "Numerical Queue Solution of Termal Noise-Induced Soft Errors in Subthreshold CMOS Devices," *ACM Great Lakes Symposium on VLSI*, May 2010. Regular presentation. Acceptance rate for regular papers 20%.

[72] C. Ferri, S. Wood, T. Moreshet, R. I. Bahar*, M. Herlihy, "Energy and Throughput Efficient Transactional Memory for Embedded Multicore Systems," *International Conference on High-Performance Embedded Architectures and Compilers.* January 2010, pp. 50-65. Acceptance rate 24%.

[73] N. Alves*, K. Nepal, J. Dworak, and R. I. Bahar, "Compacting Test Vector Sets via Strategic Use of Implications," *IEEE/ACM International Conference on Computer Aided Design*. November 2009, pp. 791-796. Acceptance rate 26%.

[74] D. Tadesse, J. Grodstein*, R. I. Bahar, "AutoRex: An Automated Post-Silicon Clock Tuning Tool," *IEEE International Test Conference*, November 2009, pp. 1-10. Acceptance rate approx. 20%.

[75] S. Reda*, A. Si, R. I. Bahar, "Reducing the Leakage and Timing Variability of 2D ICs using 3D ICs" *ACM/IEEE International Symposium on Low Power Electronics and Design,* August 2009, pp. 283-286. Acceptance rate approx. 35%.

[76] R. Le*, S. Reda, R. I. Bahar, "High Performance Cost-Effective Heterogeneous 3D FPGA Architectures," *ACM/IEEE Great Lakes Symposium on VLSI,* May 2009, pp. 251-256. Full paper presentation. Acceptance rate approx. 40%.

[77] C. Ferri*, M. Loghi, M. Poncino, R. I. Bahar, "Energy-Optimal Synchronization Primitives for Single-Chip Multi-Processors," *ACM/IEEE Great Lakes Symposium on VLSI,* May 2009, pp. 141-144. Poster presentation. Acceptance rate approx. 40%.

[78] N. Alves, K. Nepal, J. Dworak*, and R. I. Bahar, "Detecting Errors using Multi-cycle Invariance Information," *IEEE/ACM Design Automation and Test in Europe Conference*. April 2009, pp. 791-796. Acceptance rate approx. 25%.

[79] K. Nepal, N. Alves, J. Dworak*, R. I. Bahar, "Using Implications for Online Error Detection," *IEEE International Test Conference*, October 2008, pp. 1-10. Acceptance rate approx. 20%.

[80] A. Calimera, R. I. Bahar, E. Macii, M. Poncino*, "Reducing Leakage Power by Accounting for Temperature Inversion Dependence in Dual-Vt Synthesized Circuits," *ACM/IEEE International Symposium on Low Power Electronics and Design*, August 2008, pp. 217-220. Acceptance rate approx. 35%.

[81] C. Ferri*, A. Viescas, T. Moreshet, R.I. Bahar and M. Herlihy, "Energy Efficient Synchronization Techniques for Embedded Architectures," *ACM/IEEE Great Lakes Symposium on VLSI*, May 2008, pp. 435-440. Acceptance rate for regular papers approx. 30%.

[82] A. Calimera, R. I. Bahar, E. Macii*, M. Poncino, "Temperature-Insensitive Synthesis using Multi-Vt Libraries," *ACM/IEEE Great Lakes Symposium on VLSI*, May 2008, pp. 5-10. Acceptance rate for regular papers approx. 30%.

[83] D. Tadesse*, J. Grodstein, R. I. Bahar, "Fast Measurement of the `Non-deterministic Zone' in Microprocessor Debug using Maximum Likelihood Estimation," *IEEE VLSI Test Symposium*, April 2008, pp. 339-344. Acceptance rate approx. 25%.

[84] C. Ferri*, S. Reda, and R. I. Bahar, "Strategies for Improving the Parametric Yield and Profits of 3D ICs," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 2007, pp. 220-227. Acceptance rate approx. 25%.

[85] H. Li*, J. Mundy,W. R. Patterson, D. Kazazis, A. Zaslavsky, R. I. Bahar, "Thermally-induced soft errors in nanoscale CMOS circuits," *IEEE/ACM Symposium on Nanoscale Architectures(NANOARCH)*, October 2007, pp. 62-69. Acceptance rate approx. 33%.

[86] K. Nepal, R. I. Bahar*, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Techniques for Designing Noise-Tolerant Multi-level Combinational Circuits," *IEEE/ACM Design Automation and Test in Europe Conference*, April 2007, pp. 576-581. Acceptance rate approx. 25%

[87] D. Tadesse*, D. Sheffield , E. Lenge, R. I. Bahar, and J. Grodstein, "Accurate Timing Analysis using SAT and Pattern-Dependent Delay Models," *IEEE/ACM Design Automation and Test in Europe Conference*, April 2007, pp. 1018-1023. Acceptance rate approx. 25%.

[88] V. Stojanovic, R. I. Bahar, J. Dworak*, R. Weiss, "A Cost-Effective Implementation of an ECC-Protected Instruction Queue for Out-of-Order Microprocessors," *ACM/IEEE Design Automation Conference*, July 2006, pp. 705-708. Acceptance rate 20%.

[89] K. Nepal*, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Optimizing Noise-Immune Logic Circuits using Principles of Markov Random Fields," *IEEE/ACM Great Lakes Symposium on VLSI*, May 2006, pp. 149-152. Acceptance rate approx. 30%.

[90] K. Nepal*, R. I. Bahar, J. Mundy,W. R. Patterson, and A. Zaslavsky, "Designing MRF based Error Correcting Circuits for Memory Elements," *IEEE/ACM Design Automation and Test in Europe Conference*, March 2006, pp. 792-793. Interactive presentation. Acceptance rate approx. 25%

[91] T. Moreshet*, R. I. Bahar, and M. Herlihy, "Energy Reduction in Multiprocessor Systems Using Transactional Memory," *IEEE/ACM International Symposium on Low Power Electronics and Design*, August 2005, pp, 331-334. Acceptance rate 31%.

[92] K. Nepal*, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Designing Logic Circuits for Probabilistic Computation in the Presence of Noise," *IEEE/ACM Design Automation Conference*, June 2005, pp. 485-490. Acceptance rate approx. 21%

[93] Y. Bai* and R. I. Bahar, "Reducing Issue Queue Power for Multimedia Applications using a Feedback Control Algorithm," *IEEE/ACM International Conference on Computer Design*, San Jose, CA, October 2004, pp. 54-57. Acceptance rate, 37%.
[94] N. Mehta*, B. Singer, R. I. Bahar, M. Leuchtenburg, and R.Weiss, "Fetch Halting on Critical Load Misses," *IEEE/ACM International Conference on Computer Design*, San Jose, CA, October 2004, pp. 244-249. Acceptance rate for long papers 30%.
[95] K. Nepal*, H. Y. Song, R. I. Bahar, and J. Grodstein, "RESTA: A Robust and Extendable Symbolic Timing Analysis Tool," *IEEE/ACM Great Lakes Symposium on VLSI*, Boston, MA, April 2004, pp. 407-412. Acceptance rate approx. 30%.
[96] H.Y. Song*, S. Bohidar, R. I. Bahar, and J. Grodstein, "Symbolic Failure Analysis of Custom Circuits due to Excessive Leakage Current," *IEEE International Conference on Computer Design*, San Jose, CA, October 2003, pp. 70-75. Acceptance rate for long papers 26%
[97] R. I. Bahar*, J. Mundy, and J. Chen, "A Probabilistic-Based Design Methodology for Nanoscale Computation," *ACM/IEEE Proceedings of the International Conference on Computer Aided Design*, San Jose, CA, November 2003, pp. 480-486. Acceptance rate 26%.
[98] T. Moreshet* and R. I. Bahar, "Power-Aware Issue Queue Design for Speculative Instructions," *ACM/IEEE Design Automation Conference*, Anaheim, CA, June, 2003, pp. 634-637. Acceptance rate approximately 30%.
[99] Y. Bai* and R. I. Bahar, "A Dynamically Reconfigurable Mixed In-Order/Out-of-Order Issue Queue for Power-Aware Microprocessors," *IEEE Annual Symposium on Very Large Scale Integration*, Tampa, FL, February, 2003, pp. 139-146. Acceptance rate for full presentations approximately 23%.
[100] R. I. Bahar and S. Manne, "Power and Energy Reduction via Pipeline Balancing," *ACM/IEEE International Symposium on Computer Architecture*, Goteborg, Sweden, July 2001, pp. 218-229. This is the premier conference in the area of computer architecture. Acceptance rate approx. 13%.
[101] R. Maro, Y. Bai, R. I. Bahar, "Dynamically Reconfiguring Processor Resources to Reduce Power Consumption in High-Performance Processor," *Springer-Verlag Lecture Notes in Computer Science*. Vol. 2008, pp. 97–111.
[102] B. R. Fisk*, R. I. Bahar, "The Non-Critical Buffer: Using Load Latency Tolerance to Improve Data Cache Efficiency," *IEEE International Conference on Computer Design*, Austin, TX, October 1999, pp. 538-543.
[103] R. I. Bahar, G. Albera, S. Manne*, "Power and Performance Tradeoffs using Various Caching Strategies," *IEEE International Symposium on Low Power Electronics and Design*, Monterey, CA, August 1998, pp. 64–69.
[104] R. I. Bahar*, M. Burns, G. D. Hachtel, E. Macii, H. Shin, F. Somenzi, "Symbolic Computation of Logic Implications for Technology-Dependent Low-Power Synthesis," *IEEE International Symposium on Low Power Electronics and Design*, Monterey, CA, August 1996, pp. 163–168.
[105] R. I. Bahar*, F. Somenzi, "Boolean Techniques for Low Power Driven Re-Synthesis," *ACM/IEEE International Conference on Computer Aided Design*, Santa Clara, CA, November 1995, pp. 428–432.
[106] S. Manne*, A. Pardo, R. I. Bahar, G. D. Hachtel, F. Somenzi, E. Macii, M. Poncino, "On Computing the Maximum Power Cycles of a Sequential Circuit," *ACM/IEEE Design Automation Conference*, San Francisco, CA, June 1995, pp. 23–28.
[107] A. Pardo*, R. I. Bahar, S. Manne, P. Feldmann, G. D. Hachtel, F. Somenzi, "CMOS Dynamic Power Estimation Based On Collapsible Current Transistor Modeling," *IEEE International Symposium on Low Power Design*, Dana Point, CA, April 1995, pp. 111–116.

[108] R. I. Bahar*, G. D. Hachtel, E. Macii, F. Somenzi, "A Symbolic Method to Reduce Power Consumption of Circuits Containing False Paths," *ACM/IEEE International Conference on Computer Aided Design*, Santa Clara, CA, November 1994, pp. 368–371.

[109] R. I. Bahar, H. Cho, G. D. Hachtel, E. Macii*, F. Somenzi, "Timing Analysis of Combinational Circuits using ADDs," *IEEE European Conference on Design Automation*, Paris, France, February 1994, pp. 625–629.

[110] R. I. Bahar*, E. A. Frohm, C. M. Gaona, G. D. Hachtel, E. Macii, A. Pardo, F. Somenzi, "Algebraic Decision Diagrams and their Applications," *ACM/IEEE International Conference on Computer Aided Design*, Santa Clara, CA, November 1993, pp. 188–191.

d. Refereed Articles in Informal Workshops and Conferences (presenter indicated with *)

[111] Jiwon Choe*, Jonathan Lister, Tali Moreshet, Maurice Herlihy, R. I. Bahar, "Managing Concurrent Data Structures with Processing-in-Memory," *Boston Area ARCHitecture Workshop (BARC)*, January 2018.

[112] Christopher Harris*, R. Iris Bahar, "Towards the Simulation Based Design and Validation of Mobile Robotic Cyber-physical Systems," *North Atlantic Test Workshop (NATW),* May 2017.

[113] H. Tann*, S. Hashemi, R. I. Bahar, S. Reda, "Hardware-software Co-design Techniques for Deep Neural Networks," *Boston Area ARCHitecture Workshop (BARC)*, January 2017.

[114] H. Tann*, S. Hashemi, R. I. Bahar, S. Reda, "Approximate Computing in Deep Neural Networks," *Workshop on Approximate Computing*, October 2016.

[115] Fanchen Zhang*, Yi Sun, Xi Shen, Kundan Nepal, Jenifer Dworak, Theodore Manikas, Ping Gui, R. Iris Bahar, Al Crouch, John Potter, "Using Existing Reconfigurable Logic in 3D Die Stacks for Test," *IEEE North Atlantic Test Workshop*, May 2016. **Excellence in Design and Test Engineering Award** (recognizing excellence in innovative solutions to global design and test challenges)

[116] D. Papagiannopoulou*, A. Marongiu, T. Moreshet, L. Benini, M. Herlihy, R. I. Bahar, "A HTM-based Mechanism for Error -Resilient and Energy-Efficient Operation," *Boston Area ARCHitecture Workshop (BARC)*, January 2016.

[117] Marco Donato* and R. Iris Bahar, "A Fast Simulator for the Analysis of Sub-threshold Thermal Noise Transients," *Workshop on Variability Modeling*, held in conjunction with the *International Conference on Computer-Aided Design (ICCAD)*, November 2015.

[118] X. Shen, F. Zhang, Y. Sun, A. Garcia, K. Nepal, J. Dworak, R. I. Bahar, T. Manikas, P. Gui, A. Crouch, J. Potter, "Utilizing FPGAs as a Tester in 3D Stacked ICs," *IEEE International Test Conference*, Oct. 2015. Poster presentation.

[119] Thomas Carle, Dimitra Papagiannopoulou, Tali Moreshet, R. Iris Bahar, Maurice Herlihy, "A Transaction-friendly Dynamic Memory Manager for Embedded Multicore Systems," submitted to the *7th Workshop on Theory of Transactional Memory (WTTM)*, July 2015.

[120] D. Papagiannopoulou, A. Marongiu, T. Moreshet, M. Herlihy, L. Benini, R. I. Bahar, "Exploiting Transactional Memory for Error-Resilient and Energy-Efficient Execution," *Boston Area ARCHitecture Workshop (BARC)*, January 2015.

[121] Kumud Nepal, Yueting Li, R. Iris Bahar, and Sherief Reda*, "Automated High-Level Synthesis of Low Power/Area Approximate Computing Circuits," *ACM Workshop on Approximate Computing Across the System Stack (WACAS14)* March 2014.

[122] M. Donato*, R. I. Bahar, A. Zaslavsky, W. Patterson, J. Mundy, "A Synthesis Tool for Designing Noise-immune Circuits via Selectively-reinforced Logic," *IEEE Workshop on Silicon Errors in Logic – System Effects (SELSE)*, April 2014.
[123] D. Papagiannopoulou, R. I. Bahar*, T. Moreshet, M. Herlihy, A. Marongiou, L. Benini, "Transparent and Energy-Efficient Speculation on NUMA Architectures for Embedded MPSoCs," *ACM International Workshop on Manycore Embedded Systems*, June, 2013.
[124] K. Nepal, X. Shen, J. Dworak, T. Manikas, R. I. Bahar*, "Harnessing an FPGA for Built-in Self-Repair in a 3D Die Stack," *IEEE North Atlantic Test Workshop*, May 2013.
[125] G. Capodanno, D. Papagiannopoulou*, R. I. Bahar, T. Moreshet, M. Herlihy, "Embedded-SPEC: A Lightweight and Transparent Hardware Implementation of Lock Elision for Embedded Mulitcore Systems," *8th Workshop on Transactional Computing (TRANSACT)*, March 2013.
[126] Kundan Nepal*, J. Dworak, R. I. Bahar, "Detecting Delay Faults with Logic Implications," *Design Automation Conference Work-In-Progress Session*, June 2012.
[127] D. Papagiannopoulou*, P. Prasertsom, R. I. Bahar, "Flexible Data Allocation for Scratch-pad Memories to Reduce NBTI Effects," *IEEE North Atlantic Test Workshop*, May 2012.
[128] M. Donato*, P. Jannaty, Kumud Nepal, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Designing, Fabricating, and Testing Noise Immune Circuits," *2011 Subthreshold Microelectons Conference*, Sept. 2011.
[129] C. Ferri, D. Papagiannopoulou*, A. Calimera, R. I. Bahar, "NBTI-Aware Data Allocation Strategies for Scratchpad Memory Based Embedded Systems," *IEEE North Atlantic Test Workshop.* May 2011.
[130] M. Donato*, Kumud Nepal, R. I. Bahar, W. Patterson, A. Zaslavsky, J. Mundy, "Designing Noise-Immune CMOS Circuits for Sub-Threshold Operation Using Schmitt-Trigger Logic," *IEEE North Atlantic Test Symposium.* May 2011.
[131] N. Alves, Y. Shi, N. Imbriglia, J. Dworak*, K. Nepal, R. I. Bahar, "Dynamic Test Set Selection using Implication-Based On-Chip Diagnosis" *IEEE European Test Symposium*. May 2011. Accepted as poster presentation.
[132] N. Alves, K. Nepal, J. Dworak, R. I. Bahar*, "Compacting Test Vector Sets via Strategic Use of Implications," *ACM International Workshop on Logic and Synthesis (IWLS)*, July 2009.
[133] A. Calimera*, R. I. Bahar, E. Macii, M. Poncino, "Ensuring Temperature-Insensitivity of Dual -*Vt* Designs through ITD-Aware Synthesis," *IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, September 2008.
[134] N. Alves, K. Nepal, J. Dworak, R. I. Bahar*, "Detecting Multi-cycle Errors using Invariance Information," *IEEE European Test Symposium*, May 2008, (informal paper).
[135] C. Ferri*, A. Viescas, T. Moreshet, R.I. Bahar and M. Herlihy, "Energy Implications of Transactional Memory for Embedded Architectures," *Workshop on Exploiting Parallelism with Transactional Memory and other Hardware Assisted Methods (EPHAM)*, April 2008.
[136] N. Alves, K. Nepal, R. Iris Bahar, J. Dworak, "Using Implications for Online Error Detection," *IEEE North Atlantic Test Workshop*, May 2008. Informal workshop.
[137] H. Li, J. Mundy, W. R. Patterson, D. Kazazis, A. Zaslavsky, R. I. Bahar*, "Prediction of soft errors in nanoscale CMOS circuits," *Nanoelectronic Devices for Defense & Security(NANO-DDS) Conference*, June 2007.

[138] C. Ferri*, T. Moreshet, R. I. Bahar, L. Benini, and M. Herlihy, "A Framework for Supporting Transactional Memory in a MPSoC Environment," *Boston Area Architecture Workshop (BARC)*, January 2007.

[139] C. Ferri*, T. Moreshet, R. I. Bahar, L. Benini, and M. Herlihy, "A Hardware/Software Framework for Supporting Transactional Memory in a MPSoC Environment," *Workshop on Design, Architecture and Simulation of Chip Multi-Processors (dasCMP2006)*, December 2006. Held in conjunction with *IEEE/ACM International Symposium on Microarchitecture*.

[140] T. Moreshet*, R. I. Bahar, and M. Herlihy, "Energy Implications of Multiprocessor Synchronization," *ACM SPAA'06: Symposium on Parallelism in Algorithms and Architectures*, August 2006. Accepted as a transaction brief.

[141] K. Nepal*, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Techniques for MRF based implementation of multi-level combinational circuits," *IEEE Workshop on Defect and Fault Tolerant Nanoscale Architectures (NANOARCH 2006)*, held in conjunction with the *International Symposium on Computer Architecture*, June 2006.

[142] H. Li*, J. Mundy, W. Patterson, D. Kazazis, A. Zaslavsky and R. I. Bahar, "A Model for Soft Errors in the Subthreshold CMOS Inverter," *Workshop on SELSE 2, System Effects of Logic Soft Errors*, April 2006.

[143] D. Tadesse*, R. I. Bahar, and J. Grodstein, "Accurate Timing Analysis using SAT and Pattern-Dependent Delay Models," *ACM/IEEE International Workshop on Timing Issues*, February 2006. Acceptance rate 40%.

[144] T. Moreshet*, R. I. Bahar, and M. Herlihy, "Energy-Aware Microprocessor Synchronization: Transactional Memory vs. Locks," *Workshop on Memory Performance Issues*, held in conjunction with the *International Symposium on High-Performance Computer Architecture*, February 2006.

[145] V. Stojanovic*, R. I. Bahar, J. Dworak, R. Weiss, "A Cost-Effective Implementation of an ECC-Protected Instruction Queue for Out-of-Order Microprocessors," *Workshop on High Performance Computing Reliability Issues*, February 2006.

[146] T. Moreshet*, R. I. Bahar, and M. Herlihy, "Energy-Aware Microprocessor Synchronization: Transactional Memory vs. Locks," *Boston Area Architecture Workshop (BARC)*, North Kingston, RI, January 2006.

[147] B. Gojman*, V. Stojanovic, R. I. Bahar, R. Weiss, "Techniques for Fault Reduction in Out-of-Order Microprocessors," *International Workshop on Logic and Synthesis (IWLS)*, Lake Arrowhead, CA, June 2005. Acceptance rate for regular presentations, 43%.

[148] B. Gojman*, R. I. Bahar, "Dynamic Fault Prevention in Out-of-Order Processors," *Boston Area Architecture Workshop (BARC)*, Providence, RI, January, 2005.

[149] V. Stojanovic*, R. I. Bahar, R. Weiss, "When is Criticality Critical?," *Boston Area Architecture Workshop (BARC)*, Providence, RI, January, 2005.

[150] B. Singer*, N. Mehta, R. I. Bahar, R. Weiss, "Fetch Halting on Critical Load Misses," in *Workshop on Logic and Synthesis*, Temecula Creek, CA, June 2004. Acceptance rate for full presentations 42%.

[151] S. Bohidar, K. Nepal, R. I. Bahar*, "Accurate Keeper Sizing using ADD-based Models of Subthreshold Leakage," in *Workshop on Logic and Synthesis*, Temecula Creek, CA, June 2004. Acceptance rate for full presentations 42%.

[152] Y. Bai*, and R. I. Bahar, "Reducing Power with a Dynamically Reconfigurable Issue Queue," *Boston Area Architecture Workshop (BARC-2004)*, Boston, MA, January, 2004.

[153] T. Moreshet*, M. Herlihy, R. Iris Bahar, and Richard Weiss. “Reducing Power with a Dynamically Reconfigurable Issue Queue,” *Boston Area Architecture Workshop (BARC-2004)*, Boston, MA, January, 2004.

[154] J. Chen*, J. Mundy, Y. Bai, S.-M. C. Chan, P. Petrica, and R. I. Bahar, “A Probabilistic Approach to Nano-computing,” in the *2nd Workshop on Non-Silicon Computation*, San Diego, CA, June 2003.

[155] J. Chen, J. Mundy, and R. I. Bahar*, “A Probabilistic-based Design Methodology for Nanoscale Computer Architectures,” in the *Workshop on Logic and Synthesis*, Laguna Beach, CA, June 2003. Acceptance rate for full presentations 53%.

[156] E. Chi*, A. M. Salem, R. I. Bahar, and R. Weiss, “Combining Software and Hardware Monitoring for Improved Power and Performance Tuning,” *Workshop on Interaction Between Compilers and Computer Architectures*, held in conjunction with the *International Symposium on High-Performance Computer Architecture*, Anaheim, CA, February, 2003.

[157] E. Chi*, A. M. Salem, R. I. Bahar, and R. Weiss, “Combining Software and Hardware Monitoring for Improved Power and Performance Tuning,” *Boston Area Architecture Workshop (BARC-2003)*, Cambridge, MA, January, 2003.

[158] T. Moreshet and R. I. Bahar*, “Complexity-Effective Design Choices in Deeply Pipelined Processors,” *Workshop on Complexity-Effective Design*, held in conjunction with the *International Symposium on Computer Architecture*, Anchorage, AK, May 2002.

[159] H. Y. Song, R. I. Bahar*, and J. Grodstein, “Timing Analysis for Full-Custom Circuits Using Symbolic DC Formulations,” *International Workshop on Logic and Synthesis*, New Orleans, LA, June 2002. Full length presentation.

[160] H. Y. Song*, R. I. Bahar, and J. Grodstein “An ADD-Based Symbolic Analysis of Leakage Current in CMOS Circuits,” *International Workshop on Logic and Synthesis*, Lake Tahoe, CA, June 2001. Poster presentation.

[161] R. Maro, Y. Bai, R. I. Bahar*, “Dynamically Reconfiguring Processor Resources to Reduce Power Consumption in High-Performance Processor,” *Workshop on Power-Aware Computer Systems*, Cambridge, MA, November 2000. Talk presented as part of the ASPLOS conference. Submitted papers had about a 35% acceptance rate.

[162] G. Albera*, R. I. Bahar, “Power/Performance Advantages of Victim Buffer in High-Performance Processors,” *IEEE Volta International Workshop on Low Power Design*, Como, Italy, March 1999.

[163] R. I. Bahar, B. Calder, D. Grunwald*, “A Comparison of Software Code Reordering and Victim Buffers,” *Workshop on Interaction Between Compilers and Computer Architectures*, held in conjunction with the *International Conference on Architectural Support for Programming Languages and Operating Systems*, San Jose, CA, October, 1998.

[164] R. I. Bahar*, G. Albera, “Performance Analysis of Wrong-Path Data Cache Accesses,” *Workshop on Performance Analysis and its Impact on Design*, held in conjunction with the *International Symposium on Computer Architecture*, Barcelona, Spain, June, 1998.

[165] G. Albera*, R. I. Bahar, “Power and Performance Tradeoffs using Various Cache Configurations,” *Power-Driven Microarchitecture Workshop*, held in conjunction with the *International Symposium on Computer Architecture*, Barcelona, Spain, June, 1998.

[166] R. I. Bahar* “Symbolic Computation of Satisfiability and Observability Based Implications for Logic Optimization,” *IEEE North Atlantic Test Workshop*, West Greenwich, RI, May 1997, pp. 85–92.

[167] R. I. Bahar*, H. Cho, G. D. Hachtel, E. Macii, F. Somenzi, "An Application of ADD-Based Timing Analysis to Combinational Low Power Re-Synthesis," *ACM/IEEE International Workshop on Low Power Design*, Napa, CA, April 1994, pp. 39–44.

e. Guest Editor Briefs

[168] R. Iris Bahar, Alex K. Jones, and Yuan Xie, "Introduction to the Special Section on Reliable, Resilient, and Robust Design of Circuits and Systems," *ACM Transaction on Design Automation of Electronic Devices (TODAES),* Vol. 20, No. 4, Article 59, September 2015.

[169] R. I. Bahar, "Guest Editorial," *ACM Journal of Emerging Technologies in Computing (JETC)*, Vol. 5, Issue 2, Article No. 6, July 2009, pp. 6.

[170] R. I. Bahar and K. Chakrabarty, "Guest Editorial," *ACM Journal of Emerging Technologies in Computing (JETC)*, Vol. 4, Issue 2, Article No. 5, April 2008.

[171] R. I. Bahar and Stephen Edwards, "Guest Editorial," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 5, May 2006, pp. 741-742.

[172] R. I. Bahar, M. B. Tahoori, S. K. Shukla, and F. Lombardi, "Guest Editors' Introduction" Challenges for Reliable Design at the Nanoscale," *IEEE Design and Test of Computers*, Vol. 22, No. 4, July-August 2005, pp. 295-297.

g. Technical Reports

[173] H. Y. Song and R. I. Bahar, "Power, Delay, and Area Constrained Synthesis for Mixed Domino/Static Logic Optimization," Technical Report, June, 2000.

h. Patents

- *Logic Gate Size Optimization Process for an Integrated Circuit Speed Whereby Circuit Speed is Improved While Circuit Area is Optimized*, while at Motorola, Austin, TX. By Blaauw, Norton, Jones, Misra, and Bahar. U.S. patent 5,619,418, April 8, 1997.
- *Processor and Method for Delaying the Processing of Cache Coherency Transactions During Outstanding Cache Fills*, while at Digital Equipment Corp., Hudson, MA. Caching protocol for handling read/write requests from an external bus. U.S. Patent 5,404,483, April, 1995.
- *Ensuring Write Ordering Under Write-Back Cache Error Conditions*, while at Digital Equipment Corp., Hudson, MA. Protocol for properly identifying and handling cache memory hits under error conditions. U.S. Patent, September, 1994.
- *Error Transmission Mode for Multi-Processor System*, while at Digital Equipment Corp., Hudson, MA. Protocol handling of error conditions in microprocessors. U.S. Patent 5,155,843, October 13, 1992.

i. Invited Lectures and Talks

- National Institute of Standards and Technology (NIST) "Robust Object Estimation using Generative-Discriminative Inference for Secure Robotics Applications," Nov. 2018.
- Keynote Speaker, WP3 workshop. "Ventures into Low Power Computing," held in conjunction with CGO/HPCA/PPoPP, Feb. 2018.
- Panelist. "Women in Academia and Industry," Lunchtime panel during CGO/HPCA/PPoPP, Feb. 2018.

- Workshop for Women and Minorities in Computer Architecture. Panelist for session on "Preparing to Conquer to Real World," held in conjunction with the International Symposium on Microarchitecture (MICRO). Cambridge, MA. October 2017.
- Spira engineering summer camp for high school girls. Talk entitled "Computer Engineering: A Hardware-Software Challenge," July 2017.
- Annual Rhode Island Space Grant Symposium. Invited talk entitled "Accelerating image Processing Algorithms on Low-Power Embedded Platforms," April 2017.
- University of Michigan, Dept. of Computer Science and Engineering. Invited talk entitled "Accelerating Image Processing Algorithms on Low-Power Embedded Platforms," February 2017.
- Roger Williams University, invited talk entitled "Exploiting Transactional Memory for Error-Resilient and Energy-Efficient Execution on Embedded Systems, October 2016.
- Artemis computer science summer camp for high school girls. Talk entitled "Computer Engineering: A Hardware-Software Challenge," July 2016.
- Young Faculty Workshop at the ACM/IEEE Design Automation Workshop, invited talk entitled "Special Issues for New Faculty in Academia", June 2016
- Global Forum for Girls Education, panelist for session entitled "Expanding the Campus: Lincoln School's Partnerships with RISD and Brown University," February, 2016.
- MIT, Invited panelist for *Path to Professorship*. Panel entitled "Funding Your Research", November 2015. http://odge.mit.edu/development/pop/
- Karlsruhe Institute of Technology, Invited talk entitled "Exploiting Transactional Memory for Error-Resilient and Energy-Efficient Execution on Embedded Systems, October 2015.
- University of Rhode Island, Invited talk entitled "Exploiting Transactional Memory for Error-Resilient and Energy-Efficient Execution on Embedded Systems, October 2015.
- University of Massachusetts, Amherst. Invited talk entitled "Speculative Synchronization for Coherence-free Embedded NUMA Architectures," October 2014.
- Brown Club in Portland, Oregon. Invited speaker. Talk entitled "Reimagining Brown Engineering," April 2014.
- Technion Israel Institute of Technology, Haifa, Israel. Invited speaker. Talk entitled "Energy-Efficient and High-Performance Speculation Hardware for Embedded Multicore (and Many-core) Systems," June 2013.
- IEEE High-Performance Extreme Computing Conference. Invited speaker. Talk entitled "SoC-TM: Integrated HW/SW support for Transactional Memory Programming on Embedded MPSoCs," September 2012.
- Young Faculty Workshop at the ACM/IEEE Design Automation Workshop. Talk entitled "Issues for Underrepresented Groups," June 2012.
- Swarthmore College. Invited speaker. Talk entitled "Can Your Circuit Tell You When It's Failing?" November 2011.
- CRA-W/CDC Workshop on Diversity in Design Automation and Test. Invited speaker. Talk entitled "Hot Topics in Design Automation and Test", May 2011.
- Boston University. Seminar speaker. Talk entitled "Using Implications for Online Error Detection," December 2010.
- SRC Annual Review, Pittsburgh, PA. Talk entitled "Evaluating and Designing Hardware for Energy-Aware Memory Synchronization for Embedded Multicore Systems," April 2010.
- University of Massachusetts, Amherst. Seminar speaker. Talk entitled "Energy Efficient Multiprocessor Synchronization," March 2010.

- DTRA Workshop, Arlington, VA. Talk entitled "Error Prediction and Scalable Design of Error-Immune Circuitry for the Radiation Environment," January 2010.
- Young Faculty Workshop (at the Design Automation Conference), San Francisco, CA. Invited speaker. Talk entitled "Special Issues for Underrepresented Minorities," July 2009.
- University of Rhode Island. Seminar speaker. Talk entitled "SATime: A Tool for Post-Silicon Timing Validation," February 2009.
- Intel Corporation, Hudson, MA. Invited speaker. Talk entitled "Energy Efficient Synchronization Techniques for Embedded Architectures," October 2008.
- Workshop on Computer Architecture. Speaker. Talk entitled "How to Give a Good Presentation," August 2008.
- IEEE/ACM Symposium on Nanoscale Architectures (NanoArch), Anaheim, CA. Invited speaker. Talk entitled "Designing Noise-Tolerant Nanoscale Circuits based on Probabilistic Computation," June 2008.
- Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland. Invited speaker. Talk entitled "Thermal Aware Synthesis," March 2008. Talk given jointly with Enrico Macii.
- Intel Corporation, Haifa, Israel. Invited speaker. Talk entitled "Temperature Insensitive Synthesis," December 2007.
- University of Bologna, Italy. Invited speaker. Talk entitled "Designing Noise-Tolerant Logic Circuits based on Probabilistic Computation," November 2007.
- Observatoire des Micro et NanoTechnolgies, Paris, France. Invited speaker at the seminar *Nanotechnology and Complexity: Building Functionalities from Multitude*. Talk entitled "Trends and Future Directions in Nano Structure Based Computing and Fabrication," December 2006.
- Intel Corporation, Hudson, MA. Invited speaker by the Fault Aware Computing Technology (FACT) group. Talk entitled "Designing Noise-Tolerant Logic Circuits based on Probabilistic Computation," November 2006. Talk given along with my graduate student, Kundan Nepal.
- IBM Corporation, Austin, TX. Invited speaker by the Design Automation Professional Interest Committee at IBM Research. Talk entitled "Designing Noise-Tolerant Logic Circuits based on Probabilistic Computation," December 2006.
- University of Connecticut, Storrs CT. Invited speaker for Computer Science and Engineering Department colloquium. Talk entitled "Designing Noise-Tolerant Logic Circuits based on Probabilistic Computation," November 2006.
- International Conference on Computer Design, San Jose, CA. Invited speaker. Talk entitled "Trends and Future Directions in Nano Structure Based Computing and Fabrication," October 2006.
- NSF Broadening Participation in Computing Program (CRA-W / CDC Computer Architecture Summer Workshop), Princeton, NJ. Invited speaker. Talk entitled "Along the Career Path: Getting Started in Academia or Industry," July 2006.
- Foundations in Nanotechnology Conference, Snowbird, UT. Invited speaker. Talk entitled "Nanoscale Circuits and Architectures for Probabilistic Computation in the Presence of Noise," April 2006.
- Yale University, New Haven, CT. Invited speaker for the Electrical Engineering Department. Talk entitled "Designing Noise-Tolerant Circuits using Principles of Markov Random Fields," January 2006.
- IBM Corporation, Yorktown Heights, NY. Invited speaker by the Design Automation Professional Interest Committee for their seminar series. Talk entitled "Designing Noise-Tolerant Circuits using Principles of Markov Random Fields," November 2005.

- Tufts University, Medford, MA. Invited speaker for the Computer Science Department colloquium. Talk entitled, "Symbolic Methods for Accurate Timing Analysis," November 2005.
- Politecnico di Torino, Turin, Italy. Invited speaker by the computer engineering department. Talk entitled "Fetch Halting on Critical Load Misses," November 2004.
- IBM Corporation, Yorktown Heights, NY. Invited speaker by the Design Automation Professional Interest Committee for their seminar series. Talk entitled "Fetch Halting on Critical Load Misses," September 2004.
- Intel Corporation, Portland, OR. Invited speaker for their Timing Analysis Symposium. Talk entitled "Timing Analysis using Symbolic Techniques," June 2003.
- Intel Corporation, Portland, OR. Informal talk entitled "Power Aware Issue Queue Design," June 2003.
- Smith College, Northampton, MA, on "Computer Engineering at Brown," November, 2002.
- Lincoln Labs, Bedford, MA, on "Computer Engineering at Brown," August, 2002.
- Smith College, Northampton, MA, on "Power and Energy Reduction via Pipeline Balancing," November 2001.
- Analog Devices Inc., Norwood, MA, on "Power and Energy Reduction via Pipeline Balancing," November 2001.
- Brown University, Department of Computer Science, on "Performance Analysis of Wrong-Path Data Cache Accesses", February 1999.
- IBM, Yorktown Heights, NY, on "Integration of Non-Conventional CMOS Structures into Fully-Automated Synthesis Tools," March 1998.
- Northeastern University, Boston, MA, on "Symbolic Computation of Implications for Logic Optimization and Circuit Verification," April 1997.
- Mentor Graphics, Billerica, MA, on "Symbolic Computation of Implications for Logic Optimization and Circuit Verification," March 1997.
- Digital Equipment Corporation (Digital Semiconductor), Hudson, MA, on "Symbolic Computation of Logic Implications for Technology-Dependent Low-Power Synthesis," January 1997.
- Brown University Department of Computer Science Seminar Speaker, October, 1996.
- University of Rhode Island Electrical and Computer Engineering Department Seminar Speaker, September, 1996.
- Dagstuhl Seminar on Computer-Aided Design and Test, Dagstuhl, Germany, February, 1995.

j. Work in Progress

- *Energy Efficient Transactional Memory Techniques for Embedded Architectures*
  Because many embedded devices run on batteries, *energy efficiency* is perhaps the single most important criterion for evaluating hardware and software effectiveness in embedded devices. In this project, we have looked into developing energy-efficient implementations using hardware transactional memory (HTM) on an embedded platform. We also explored implementing more effective memory allocation methods that may be used on top of HTM. A new aspect of this work includes exploring how the HTM framework can be used to support error recovery and approximate results caused by aggressive use of voltage over-scaling. This work has being supported by NSF.

- *Concurrent Processing-in-Memory Architectures*
  A *Processing-In-Memory* (PIM) architecture consists of one or more simple processors each with its own memory. PIM modules are best viewed as *accelerators*, providing

powerful yet specialized enhancements to existing systems running existing software. This project has the dual aim of adapting highly-concurrent data structures to PIM architectures, and of adapting PIM architectures to the needs of today's concurrent software.

- *Modeling Thermal Noise Effects in Nanoscale Circuits and Designing Noise Tolerant Circuits*
  Electrical noise will play an increasingly critical role in future nanoscale CMOS circuit operation characterized by lower supply voltages and smaller device sizes. Both of these downscaling approaches reduce the margin of immunity to thermal noise, alpha particle strikes, and threshold voltage variations. This project focuses on developing new modeling techniques to capture transient noise effects due to thermal and RTS noise. In addition, we are exploring new approaches for noise-immune circuit design. This work is supported by NSF.

- *Robust Robot Perception*
  The goal of this project is to implement new algorithms in hardware and software to support accurate and energy-efficient robot perception. In particular, perception is a critical capability to enable purposeful goal-directed manipulation for autonomous robots. Object detection and recognition techniques used for robot perception have greatly improved over the past few years. However, these improvements have often come at the expense of significant energy consumption and computational inefficiency. In order to achieve real-time energy-efficient computing for these autonomous robots, we need to rethink not just the perception algorithms themselves, but also how they are implemented in hardware and the computational resources allocated to their execution.

- *Design of Hardware/Software Techniques for Efficient Stereo Matching Algorithms*
  Visual stereo matching of images is of limited value when weather conditions offer zero visibility. Instead, there is a reliance on using infrared cameras to match visual images taken at a previous time, under good weather conditions. Gradient-based cross-spectral stereo matching (GB-CSSM) is used to create disparity maps to compare images for accurate identification. However, there is a need to improve upon existing techniques, both in terms of runtime and accuracy. The goal of this project is to implement new algorithms that generate detailed-rich disparity maps in real-time that can be applied under a range of environmental conditions. Funding for the project is through Draper Lab.

- *Techniques for Built-in Self-Repair in 3D Die Stacks Using Programmable Logic*
  Three-dimensional stacked integrated circuits (ICs) hold much promise for increasing system performance. However, they are also difficult to test and assemble, leading to yield issues. This project investigates the use of unused (or underused) resources within the 3D stack to replace defective portions of a die. In particular, we are exploring techniques for error detection, different levels of granularity for replacement, and optimal use of reconfigurable logic to repair the errors. This work has been supported in the past by NSF.

6. Research Grants

a. Current Grants:

- NSF grant entitled "Effects of Small-scale Noise in Ultimate CMOS: Simulation Frameworks, Noise-Immune Circuit Designs, and Experimental Validation," Principal investigators: R. I. Bahar (PI), A. Zaslavsky, and W. R. Patterson. Total amount: $360,000, over 3 years.

b. Completed Grants:

- Draper Graduate Student Fellowship for PhD student Christopher Picardo. Tuition and stipend for 4 years. Draper Laboratory.
- NSF grant entitled "Automatic High-Level Synthesis of Approximate Computing Circuits," Principal investigators: S. Reda (PI) and R. I. Bahar. Total amount: $449,998 over 3 years.
- NSF grant entitled "Collaborative Research: Transparent and Energy-Efficient Speculation on NUMA Architectures for Embedded Multiprocessor Systems," Principal investigators: R. I. Bahar (PI) and T. Moreshet (Swarthmore). Award amount: $500,000, over 3 years.
- NASA grant entitled "Web-scale Assisted Robot Teleoperation," with Peter Schulz and Christopher Roman (URI). Amount to Brown: $250,000 (approx.), over 2 years.
- NSF REU supplement for summer 2016 from NSF-CSR grant. Total amount: $7,000 over 10 weeks.
- Brown University Global Mobility Graduate Research Fellowship entitled "Exploiting Transactional Memory for Error-Resilient and Energy-Efficient Execution on Embedded Systems," to support PhD dissertation work in Switzerland for Dimitra Papagiannopoulou. Total amount: $9,000 over 3 months.
- Brown Seed grant "Enabling Autonomous Flight of Drones in Complex, Unpredictable Environments," Principal investigators: R. I. Bahar (PI), S. Reda, J. Kellner, O. C. Jenkins. Total amount: $80,000 over 12 months.
- Brown University UTRA grant entitled "Enabling Autonomous Flight of Drones in Complex, Unpredictable Environments," Principal investigators: Adam Gosselin (student), R. I. Bahar (faculty advisor). $3500 over 10 weeks.
- DTRA/ONR option year grant request entitled "Design Science for Radiation-Effects Rate Prediction and Development of Error-Immune Circuitry," Principal investigators: R. I. Bahar (PI), A. Zaslavsky, J. Mundy, and W. Patterson, R. Schrimpf, R. Weller, R. Reed, M. Alles, B. Bhuva. March 2013. Award amount: $350,000, over 1 year. Note: this was supposed to be a $700,000 award for a 2-year option extending our prior DTRA award. However, the due to budgetary constraints within DTRA, the final year of funding was cut after the award was made.
- ARO/ONR/AFOSR equipment grant entitled "DURIP: An Infrared System for Thermal-Driven Research in Computer Vision" Principal investigators: S. Reda, R. I. Bahar, and J. Mundy. Award date: March 2009. Award amount: $126,590.
- NSF grant entitled "Collaborative Research: Energy-Aware Memory Synchronization for Embedded Multicore Systems," Principal investigators: R. I. Bahar (PI), M. Herlihy, and T. Moreshet. Award date: August 2009. Award amount: $286,643 (with $244,262 going to Brown University) over 3 years.
- NSF grant number CCF-0915302 entitled "SHF: Small: Collaborative Research: Using Identified Circuit Invariance for Online Error Detection", Principal investigators: J. Dworak (PI), R. I. Bahar, and K. Nepal. Award date: August 2009. Award amount: $476,813 over 3 years.
- DTRA/ONR grant entitled "Design Science for Radiation-Effects Rate Prediction and Development of Error-Immune Circuitry," Principal investigators: R. I. Bahar (PI), A.

Zaslavsky, J. Mundy, and W. Patterson, R. Schrimpf, R. Weller, R. Reed, M. Alles, B. Bhuva. Award date: March 2010. Award amount: $1,050,000 over 3 years.

- DoD SBIR Phase I grant entitled "Processing of Large Wide Area Airborne Sensor Data Streams in Hardware," Principal investigators: R. I. Bahar (PI) and S. Reda. Award date: March 2012. Award amount: $50,000 over 1 year.
- SRC grant entitled "Collaborative Research: Energy-Aware Memory Synchronization for Embedded Mulicore Systems," Principal investigators: R. I. Bahar (PI) and M. Herlihy Award date: June 2010. Award amount: $90,000 over 3 years. (part of a joint NSF/SRC grant).
- DARPA subcontract grant entitled "Wide Area Video Motion Blur Elimination" Principal investigators: R. I. Bahar (PI), J. Mundy and S. Reda. Award date: March 2010. Award amount: $180,000 over 2 years.
- NSF REU grant entitled "Collaborative Research: Energy-Aware Memory Synchronization for Embedded Mulicore Systems," Principal investigators: R. I. Bahar (PI), M. Herlihy. Award date: July 2010. Award amount: $14,630 over 3 months.
- NSF supplementary grant to support the Design Automation Summer School, a 2-day summer school featuring lectures by 7 experts involved in various areas of research related to electronic design automation. Intended for graduate students in their first or second year of studies in electronic design automation. Award amount: $10,000.
- NSF grant under Nanotechnology Interdisciplinary Research Teams (NIRT) entitled "NIRT: Fault-tolerant, Probabilistic Computing with Markov Random Field Architectures and CMOS Nanodevices" Principal investigators: R. Iris Bahar, Joseph Mundy, William Patterson, and Alexander Zaslavsky. Award date: September 2005. Award amount: $317,000 over 4 years (extended an extra year).
- CRAW-CDC Grant entitled "Computer Architecture Summer School: Getting Undergraduates Excited about Research." Principal organizers: R. I. Bahar, Margaret Martonosi (Princeton University), Russ Joseph (Northwestern University), Kunle Olukotun (Stanford University). Award date: February 2008. Award amount: $30,000 to support a 2-day summer workshop targeted at getting women and underrepresented minorities interested in research in computing.
- Brown Career Development Award to support new collaboration efforts with Prof. Metra at the University of Bologna. PIs: Jennifer Dworak and R. I. Bahar. Award date: April 2007. Award amount: $8,685 for 1 year.
- NSF Grant under Broadening Participation in Computing entitled "Widening the Research Pipeline." To implement and evaluate programs to increase the participation of women and minorities in computing research. Award date: June 2006. Award amount: $1,499,999 over 3 years.
- Intel Corporation grant entitled "Fast, Accurate Symbolic Timing Analysis for Custom Circuits." Principal investigator, R. Iris Bahar. Award date: October 2004. Award amount: $75,000 over 3 years (awarded in 3, $25,000 allotments).
- Undergraduate Teaching and Research Assistantship (UTRA) for a collaborative project with Briant Mairs and Prof. Jennifer Dworak entitled "Redundant Circuitry Generation using Fault Tolerance Testing Tools" June–August 2007. Award amount: $2500.
- NSF Grant in the area of Computer Systems Architecture entitled "Combining Hardware and Software Monitoring for Improved Power and Performance Tuning" Principal investigators, R. I. Bahar and R. Weiss. Award date: August 2003. Award amount: $160,000 over 3 years.
- NSF Grant in the area of Design Automation entitled "Using Symbolic DC Analysis to Evaluate Complex Custom Circuit Designs." Principal investigator, R. I. Bahar. Award date: July 2002. Award amount: $160,000 over 4 years.

- NSF Grant under Nanotechnology Exploratory Research entitled "NER: Exploring Nanodevices for Probabilistic Computing Architectures." Principal investigators: Alexander Zaslavsky, R. Iris Bahar, Jie Chen and Joseph Mundy. Award date: August 2004. Award amount: $100,000 over 2 years.
- NSF Grant in the area of Nanotechnology Exploratory Research entitled "NER: Y-Junction Nanotube-based Computer Devices and Architectures" Principal investigators, R. Iris Bahar, Jie Chen and Joseph Mundy. Award date: July 2003. Award amount: $100,000 over 2 years.
- Microsoft Grant for Course Development. This grant was used to purchase and test out new Windows-based layout tools for EN160 (VLSI System Design). Up to now, the software for EN160 has all been Unix-based. Principal investigator, R. I. Bahar. Award date: August 2003. Award amount: $5,000 over 1 year.
- Microsoft Grant for Teaching and Research. The goal of this grant was to become familiar with Windows-based real-time operating systems by using it for operating a life-like robotic head for speech recognition experiments. Principal investigators, R. I. Bahar and H. Silverman. Award date: June 2003. Award amount: $25,000 over 1 year.
- Collaborative Research Award from SUN Microsystems, Inc. "Expanding Teaching and Research Activities in VLSI System Design and Computer Architecture." Principal investigator, R. I. Bahar. Award date: December 2000. Award amount: Over $300,000 worth of equipment.
- NSF Early Career Development Grant (CAREER) proposal entitled "(Re)Configurable Architectures for High Performance and Low Power." Principal investigator, R. I. Bahar. 6/98–5/03. Award amount: $214,000.
- NSF Professional Opportunities forWomen in Research and Education (POWRE) proposal entitled "Integration of Non-Conventional CMOS Structures into Fully-Automated Synthesis Tools." Principal investigator, R. I. Bahar. 9/98–5/00. Award amount: $75,000.
- Equipment Grant from Digital Equipment Corporation. The hardware was granted to Brown as a classroom teaching tool or for other research and experimentation purposes. The "kit" is based on DEC's Alpha technology and contains the CPU, Motherboard and the Design Kit. Award date: May 1998.
- RichSalomon Faculty Research Award for the proposal entitled "Low-Power VLSI: Designs for the Future." 9/97–5/98. Award amount: $14,500.
- Design Automation Graduate Scholarship for the proposal entitled "Using Implications to Drive Low-Power Optimization of Technology-Dependent Circuits," sponsored by the Design Automation Conference. 9/97–5/98. Award amount: $12,000.
- Undergraduate Teaching and Research Assistantship for a collaborative project with Brad Simeral. The project is entitled "Computer System Design Laboratory: Building Systems Using Today's Technology." June–August 1997. Award amount: $2,200.

7. Service

a. University

- Freshman application review committee, 1996, 1998, 1999.
- Freshman advisor, 1997–1999, 2002–2007, 2008-2014, 2016.
- Student Chapter of the IEEE faculty advisor, 1996–1998, 2004.
- Committee member on the Status of Women, 1997–2000.

- Advisor for the Engineering A.B. Program, 1998–2002.
- Advisor for the Computer Engineering concentration, Spring 2000, 2003, 2005.
- Graduate representative for the Electrical Sciences and Computer Engineering Group, 2003–2006, 2010/11.
- Graduate Council Member, 2004–2006.
- Faculty Search Committee Chair for Computer Engineering, 2004, 2006, 2010/11, 2011/12.
- Search Committee member for the new Dean of the School of Engineering, 2010/11.
- Member of the Engineering Executive Committee, 2006-2007, 2008-2010.
- Director of Undergraduate Programs (Division of Engineering), 2006-2007, 2008-2010.
- Randall Advisor, 2010-2013.
- Co-Chair for the University Strategic Committee on Reimaging Campus, 2012/2013
- Vice Chair, Chair, Past-Chair of the Faculty Executive Committee, 2012-2015
- Participant in TEAM: Team Enhanced Advising and Mentoring, 2013/2014
- Provost Search Committee, 2014
- Chair of the Community Planning Committee for the new School of Engineering building, 2014-2017.
- School of Engineering Concentration Chair, 2014/15
- Initiated *Introduction to Engineering* course for high school girls at the Lincoln School (taught 4 years, 2015-2019)
- School of Engineering "Brown Engineering Alumni Medal" (BEAM) selection committee, 2012-2019.
- Member of the University Tenure, Promotion, and Appointments Committee (TPAC), 2016-1019.

b. Profession

- Senior Member of the Institute of Electrical and Electronic Engineers (IEEE).
- Distinguished Scientist of the Association for Computing Machinery (ACM).
- Executive Committee Member for the Associate of Computing Machinery special interest group on design automation (SIGDA)
- Member of Sigma Xi (Scientific Research Society).
- Reviewer for various Journals and Conferences, including *IEEE Transactions on Computer-Aided Design*, *ACM Transactions on Design Automation of Electronic Systems, ACM/IEEE Design Automation Conference, ACM/IEEE International Conference on Computer-Aided Design*, *ACM/IEEE International Symposium on Microarchitecture, ACM/IEEE Symposium on Computer Architecture*
- Proposal Reviews: Panelist and individual proposal reviewer for NSF and ONR/DTRA
- Program Committee Member for various conferences, including *IEEE International Symposium on Low-Power Electronics and Design, ACM/IEEE Design Automation and Test in Europe,* ACM/IEEE Symposium on High-Performance Computer Architecture, *ACM/IEEE International Symposium on Nanoscale Architectures*, *ACM/IEEE Design Automation Conference, ACM/IEEE International Conference on Computer-Aided Design*
- Chair and Editor positions
  - *ACM International Conference on Architectural Support for Programming Languages and Operating Systems,* General Chair, 2019.

- *IEEE/ACM International Conference on Computer-Aided Design,* Executive Committee Member (Workshop chair, Special Session Chair, Program Chair, General Chair), 2012-2018.
- *IEEE Networks, Architecture, and Storage Conference*, Technical Program Chair, 2015.
- *ACM Transactions on Embedded Systems,* Associate Editor, 2014-2016.
- *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, Associate Editor, 2006-2013.
- *IEEE Transactions on VLSI Systems*, Associate Editor, 2009-2013.
- Executive Committee Member (Education Chair) for the Association for Computing Machinery (ACM) Special Interested Group on Design Automation (SIGDA), (vice-chair, 2012/2013), 2010-2013.
- *ACM Journal of Emerging Technologies in Computing*, Associate Editor, 2007-2010.
- *ACM/IEEE Great Lakes Symposium on VLSI,* Program Co-Chair 2009, General Chair 2010.
- *ACM/IEEE MICRO Symposium,* Workshop co-Chair 2009.
- *ACM Symposium on Nanoarchitecture,* Program Chair, 2010.
- *IEEE/ACM International Conference on Computer-Aided Design,* Executive Committee Member and "Nano-chair", 2007/8, 2014-2017.
- *ACM Transactions on Design Automation of Electronic Systems*, Guest Editor for special issue on "Best of Nano at ICCAD 2006", published April 2008.
- *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, Guest Editor for special issue on "Best of IWLS 2005", published April 2006.
- *IEEE Design & Test of Computers*, Guest Editor for special issue on Advanced Technologies and Reliable Design for Nanotechnology Systems, July–August 2005.
- Workshop organizer, *Exploiting Nanoscale Devices for Future Computing*, held in conjunction with the *International Conference on Computer-Aided Design (ICCAD)*, November 2005.
- *IEEE/ACM Workshop on Logic and Synthesis*, Technical Program Chair 2005. General Chair 2006.
- *Boston Area Architecture Workshop*, Workshop Chair, 2005.

8. Academic Honors, Fellowships, Honorary Societies

a. Promoted to Full Professor, effective July 2012.
b. Distinguished Scientist Award from the Association of Computing Machinery (ACM), awarded 2012.
c. Senior Membership of the IEEE, awarded 2012.
d. Promoted to Associate Professor, effective July 2003.
e. Patricia Robert Harris Fellowship, 1992–1995.
f. Eta Kappa Nu, Electrical Engineering Honor Society, since 1985.
g. Tau Beta Pi, Engineering Honor Society, since 1985.

9. Teaching

a. Regular Courses:

- EN0520: Electrical Circuits and Systems, 2000, 2001.

- EN1600: Design and Implementation of VLSI Systems, 2003-05, 2010-11, 2014, 2016.
- EN1640: Design of Computing Systems, 1996–1999, 2006, 2007, 2009, 2015.
- GISP-20: Advanced VLSI Design, 1997.
- EN2910W, Synthesis of VLSI Systems, 1996, 1997, 2002.
- EN2910A: Advanced Computer Architecture, 1998, 2002, 2004, 2006.
- EN2910P: Nanosystem Design, 2003, 2005.
- EN2912E: Low Power VLSI System Design, 2008, 2012, 2014, 2017.
- EN0030: Introduction to Engineering, 2009, 2010, 2011, 2012.
- EN1931I: Introduction to Robot Design, 2017, 2018.
- ENGN1630: Digital Electronics System Design, 2018.

b. Undergraduate Independent Study:

Ernest Lampe, Greg Pomerantz, Brad Simeral, Joshua Fredericks, Rany Ng, Dale Bertrand, Mahesh Madhav, Tom Duffy, Samir Gupta, James Harris, Justin Permar, Erika Tate, Jessica Riggs, Julia Cline, Eric Chi, Michael Salem, Saswat Bohidar, Brian Singer, Mark Johnson, Benjamin Gojman, Martin Voeller, Muhammad Zulkifli, David Sheffield, Bryant Mairs, Gregory Howard, Samantha Wood, Chris Moynahan, Patipan Prasertsom, Warren Jin, Lauren Moser, Adam Gosselin, Sungseob Whang, Tymani Rachford, Christopher Casares, Kevin Anderson.

c. B*achelor's Honors Theses:*

- Ernest Lampe, Greg Pomerantz, Brad Simeral, Josh Fredericks, Mahesh Madhav, Jessica Riggs, Julia Cline, Eric Chi, Saswat Bohidar, David Sheffield, Gregory Howard, Warren Jin, Lauren Moser, Sungseob Whang, Christopher Casares.

d. Master's Theses:

- D'Sunte Wilson, May 1998
- Brian Fisk, July 1999
- Roberto Maro, December 2000 (in collaboration with the Politecnico di Torino, Italy)
- Tali Moreshet, August 2002 (continuing Ph.D. student)
- Marco Donato, October 2010 (in collaboration with La Sapienza, Rome)
- Fabio Cremona, May 2012 (in collaboration with La Sapienza, Rome)
- Giuseppe Capodanno, October 2012 (in collaboration with La Sapienza, Rome)
- Xijun Han, May 2016
- Francesco Buttafuoco, February 2018 (in collaboration with Politecnico di Torino, Italy)
- Giselle Garcia, May 2018

e. Ph.D. Theses:

- Yu Bai, August 2004
- Hui-Yuan Song, September 2005
- Tali Moreshet, May 2006 (co-advised with Maurice Herlihy)
- Kundan Nepal, May 2007
- Desta Tadesse, May 2009
- Cesare Ferri, May 2011 (co-advised with Maurice Herlihy)
- Roto Le August 2012 (co-advised with Joe Mundy)
- Kumud Nepal, May 2015 (co-advised with Sherief Reda)
- Onur Ulusel, May 2016
- Marco Donato, May 2016

- Dimitra Papgiannopoulou, May 2016
- Christopher Picardo, May 2018

f. Master's Non-Thesis:

- Daniel Goldwater, May 1998
- Brad Simeral, May 1999
- Andrew Mirsky, James Harris, May 2001
- Dale Bertrand, Mahmoud Ben-Naser, May 2002.
- Kevin Wong, May 2003.
- Yu Bai, May 2004 (continued as Ph.D. student)
- Alana Fu, Kierstan Bell, May 2005
- Vladimir Sojanovic, Hua Li, May 2006
- Cesare Ferri, May 2008 (continuing Ph.D. students)
- Roto Le, May 2009 (continuing Ph.D. student)
- Nuno Alves, May 2010
- Kumud Nepal, May 2011 (continuing Ph.D. student)

g. Current Ph.D. Students:

- Jiwon Chou (co-advised with Maurice Herilhy, expected 2021)
- Yanqi Liu (expected 2022)

h. Postdoctoral advisees:

- Thomas Carle, 2014-2015
- Christopher Harris, 2015-2017
- Dimitra Papagiannopoulou, 2016-2017
- Marco Donato, 2016

10. Personal

Citizenship: United States of America
Gender: Female
Ethnicity: White

11. Date Document Prepared

December 2018