Sherief M. Reda – Curriculum Vitae

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Legal Name: Sherief M. Reda El-Edel

1. CONTACT INFORMATION

School of Engineering
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2. EDUCATION

- Ph.D. in Computer Science and Engineering, University of California, San Diego, 2001 – 2006.
  Thesis title: *New Approaches for Placement and Benchmarking of CMOS and Gene Chips*.
  Thesis advisor: Professor Andrew B. Kahng.
- M. Sc. in Electrical and Computer Engineering, Ain Shams University, Cairo, Egypt, 1998 – 2000.
  Thesis title: *Combinational Equivalence Checking*.
  Thesis advisor: Professor Ashraf Salem.
- B. Sc. Distinction (magna cum laude) in Electrical / Computer Engineering, Ain Shams University, Cairo, Egypt, 1998.

3. RESEARCH INTERESTS

Broad interests in computer engineering areas including energy-efficient computing, electronic design automation, embedded systems, computer architecture and reconfigurable computing.

Current research projects:

- Approximate computing design paradigms.
- Energy-efficient processing for embedded deep learning, biometric security systems, and image/video applications.
- Power/thermal sensing and modeling for SoCs and for security applications.
- Power/thermal adaptive management for mobile SoCs and HPC clusters.
- Emerging molecular informatics storage and processing systems.

4. WORK EXPERIENCE

- **Full time positions:**
  - Associate Professor (with tenure) of Engineering, Brown University (July 2013 –). CS appointment in July 2016.
  - Assistant Professor of Engineering, Brown University (July 2006 – June 2013).
  - Teaching/Research Assistant, University of California, San Diego (Spring 2001 – Spring 2006).
  - Teaching/Research Assistant, Ain Shams University, Cairo, Egypt (Fall 1998 – Fall 2000).
- **Consulting Experience:**

- Fish & Richardson law firm. Expert witness on power management techniques for processors.

- **Visiting and part-time positions:**
  - Visiting scholar at Harvard School of Engineering and Applied Sciences (Spring 2015 sabbatical).
  - Intel Design and Technology Group, Santa Clara (Summer 2005).
  - IBM Austin Research Laboratory, Austin, Texas (Summer 2004).
  - TIMA Laboratory, Grenoble, France (Summer 2000).
  - Mentor Graphics Corporation, Cairo, Egypt (Fall 1998 – Fall 2000).

5. AWARDS AND RECOGNITIONS

2016 National Academy of Sciences (NAS) US Arab Fellowship.

2015 Best Paper Nomination, International Conference on Computer-Aided Design (ICCAD)

2014 Elevated to IEEE Senior status

2013 Promoted to associate professor with tenure

2010 Best Paper Award, International Symposium on Low-Power Electronic Design (ISLPED) (2 out of 203 papers)

2010 DAC A. Richard Newton award (1 out of 20 proposals)

2010 National Science Foundation CAREER award

2008 Best Paper Nomination, Asian South-Pacific Design Automation Conference (ASPDAC) (10 out of 350 papers)

2008 Brown University Richard B. Salomon Award

2005 Best Paper Nomination, International Conference on Computer-Aided Design (ICCAD)

2005 First Place Award, VLSI placement contest, ACM International Symposium on Physical Design (ISPD) (1 out of 9 teams)

2005 "Hot" (most downloaded) article in Operations Research Letters

2004 Best Poster Award, UCSD Jacobs School of Engineering Research Review Expo (10 out of 200 posters)

2003 Best Poster Award, UCSD Jacobs School of Engineering Research Review Expo (10 out of 180 posters)

2002 Best Paper Award, Design Automation and Test in Europe Conference (DATE) (3 out of 476 papers)

2001 Cal-$(IT)^2$ fellowship, University of California, San Diego

1998 First rank of graduating class among all engineering departments, Ain Shams University, Cairo, Egypt

1993 High school valedictorian, El-Nasr English School, Cairo, Egypt

6. PUBLICATIONS (H-INDEX=28)

– Earlier publications coauthored with Ph.D advisor, Prof. A. B. Kahng, have their authors listed in alphabetical order.

Books

[1] S. Reda and A. N. Nowroz, "Power Modeling and Characterization of Computing Devices: A Survey," Foundations and Trends in Electronic Design Automation, NOW Publishers, 2012. `https://www.amazon.com//dp/1601985606`

[2] S. Reda and M. Shafique (Eds), "Approximate Computing: Circuits and Methodologies", Springer, 2018 (to appear).

Book Chapters

[1] A. B. Kahng and S. Reda and Q. Wang, "APlace: A High Quality, Large-Scale Analytical Placer," *Modern Circuit Placement: Best Practices and Results*, Springer, 2007, J. Cong and G-J. Nam (ed.), pp. 163 – 187.

[2] A. B. Kahng, I. Măndoiu, S. Reda, A. Zelikovsky and X. Xu, "Computer-Aided Optimization of DNA Array Design and Manufacturing," *Design Automation Methods and Tools for Microfluidics-Based Biochips*, Springer, 2006, K. Chakrabarty (ed.), pp. 253 – 269.

[3] A. B. Kahng and S. Reda, "Digital Layout - Placement," *The CRC Handbook of EDA for IC Design*, CRC Press, 2005, G. Martin and L. Lavagno (ed.), Vol. 2., pp. 5.1 – 5.23.

[4] H. Tann, S. Hashemi, F. Buttafuoco, and S. Reda, "Approximate Computing for Iris Recognition Systems", to appear in *Approximate Computing: Circuits and Methodologies*, Springer, 2018.

[5] S. Hashemi, H. Tann and S. Reda, "Approximate Logic Synthesis Using Boolean Matrix Factorization", to appear in *Approximate Computing: Circuits and Methodologies*, Springer, 2018.

Papers in Archival Proceedings and Journals

– Journals marked with **J**.

[1] C. Rose, S. Reda, B. Rubenstein and J. Rosensetin, "Computing With Chemicals: Perceptrons Using Mixtures of Small Molecules", to appear in *IEEE International Symposium on Information Theory*, 2018.

[2] S. Hashemi, H. Tann and S. Reda, "BLASYS: Approximate Logic Circuit Synthesis Using Boolean Matrix Factorization," to appear in *IEEE/ACM Design Automation Conference* (**DAC**), 2018.

[3] S. Hashemi, H. Tann, F. Buttafuoco and S. Reda, "Approximate Computing for Biometric Security Systems: A Case Study on Iris Scanning," to appear in *IEEE Design, Automation Test in Europe* (**DATE**), 2018. Acceptance Rate 23.7%.

[4] M. Nabavinejad,, X. Zhan, R. Azimi, M Goudarzi, and S. Reda, "QoR-Aware Power Capping for Approximate Big Data Processing," to appear in *IEEE Design, Automation Test in Europe* (**DATE**), 2018.

[5] **J** S. Reda, K. Dev and A. Belouchrani, "Blind Identification of Thermal Models and Power Sources from Thermal Measurements ," in *IEEE Journal on Sensors*, 2018.

[6] **J** K. Dev, X. Zhan and S. Reda, "Scheduling on CPU+GPU Processors under Dynamic Conditions," in Journal on Low-Power Electronics (**JOLPE**), American Scientific Publishers, 2017.

[7] S. Steffl and S. Reda, "LACore: A Supercomputing-Like Linear Algebra Accelerator for SoC-Based Designs," in IEEE Conference on Computer Design (**ICCD**), pp. 137-144, 2017. Acceptance rate 29%.

[8] **J** S. Reda, "3D Integration Advances Computing", **Nature**, Vol. 547, pp. 38-40, July 2017. (invited in News & Views Section)

[9] R. Azimi, T. Fox and S. Reda, "Understanding the Role of GPGPU-accelerated SoC-based ARM Clusters", in IEEE Cluster (**Cluster**), pp. 333-343, 2017. Acceptance rate 21.8%.

[10] M. Shalan and S. Reda, "CloudV: A Cloud-Based Educational Digital Design Environment," IEEE International Conference on Microelectronic Systems Education (MSE), pp. 39 - 42, 2017.

[11] F. Kaplan, S. Reda and A. Coskun, "Fast Thermal Modeling of Liquid, Thermoelectric, and Hybrid Cooling", in IEEE The Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (**iTherm**), pp. 726 – 735, 2017.

[12] H. Tann, S. Hashemi, R. I. Bahar and S. Reda, "Hardware-Software Codesign of Highly Accurate, Multiplier-free Deep Neural Networks", in *IEEE/ACM Design Automation Conference* (**DAC**), pp. 28:1-28:6, 2017.

[13] R. Azimi, M. Badiei, L. Na and S. Reda, "Fast Decentralized Power Capping for Server Clusters", *in IEEE Symposium on High-Performance Computer Architecture* (**HPCA**), pp. 181-192, , 2017. Acceptance rate 22%.

[14] S. Hashemi, N. Anthony, C. Tann, R. I. Bahar and S. Reda, "Understanding the Impact of Precision Quantization on the Accuracy and Energy of Neural Networks", in IEEE/ACM Design, Automation & Test in Europe (**DATE**), pp. 1474-1479, 2017.

[15] S. Reda and A. Belouchrani, "Blind Identification of Power Sources in Multicore Processors", in IEEE/ACM Design, Automation & Test in Europe (**DATE**), pp.1739-1744, 2017.

[16] K. Dev, X. Zhan and S. Reda, "Power-Aware Characterization and Mapping of Workloads on CPU-GPU Processors", in IEEE International Symposium on Workload Characterization (**IISWC**), pp. 225-226, 2016.

[17] **J** K. Nepal, S. Hashemi, C. Tann, R. I. Bahar and S. Reda, "Automated High-Level Generation of Low-Power Approximate Computing Circuits", in IEEE Transactions on Emerging Topics in Computing, 2016.

[18] **J** X. Zhan, R. Azimi, S. Kanev, D. Brooks and S. Reda, "CARB: A C-State Power Management Arbiter For Latency-Critical Workloads", in IEEE Computer Architecture Letters (**CAL**), 16(1): 6-9, 2016.

[19] C. Tann, S. Hashemi, R. I. Bahar and S. Reda, "Runtime Configurable Deep Neural Networks for Energy-Accuracy Trade-off", in *IEEE International Conference on Hardware/Software Codesign and System Synthesis* (**CODES**), 34:1-34:10, 2016.

[20] K. Dev and S. Reda, "Scheduling Challenges and Opportunities in Integrated CPU+GPU Processors ", in ACM/IEEE Symposium on Embedded Systems for Real-time Multimedia (**ESTI**), pp. 78-83, 2016.

[21] Ulusel, C. Picardo, C. Harris, S. Reda and R. I. Bahar, "Hardware Acceleration of Feature Detection and Description Algorithms on Low-Power Embedded Platforms", in *IEEE Field Programmable Logic* (**FPL**), pp. 1-9, 2016.

[22] K. Dev, S. Reda, I. Paul, W. Huang and W. Burleson, "Workload-aware Power Gating Design and Run-time Management for Massively Parallel GPGPUs", *in IEEE Symposium on Very-Large Scale Integration* (**ISVLSI**), pp. 242-247, 2016.

[23] S. Hashemi, R. I. Bahar and S. Reda, "A Low-Power Dynamic Divider for Approximate Applications", in *IEEE/ACM Design Automation Conference* (**DAC**), 105:1-105:6, 2016.

[24] X. Zin, M. Shoaib and S. Reda, "BXplore: Creating Soft Heterogeneity in Clusters Through BIOS Re-configuration", in *IEEE Cluster, Cloud and Grid Computing* (**CCGRID**), 540-549, 2016.

[25] M. Badiei, X. Zhan, R. Azimi, S. Reda and N. Li, "DiBA: Distributed Power Budget Allocation for Large-Scale Computing Clusters", in *IEEE Cluster, Cloud and Grid Computing* (**CCGRID**), pp. 70-79, 2016.

[26] **J** X. Zhan and S. Reda, "Power Budgeting Techniques for Data Centers", IEEE Transactions on Computers, Vol. 64(8), pp. 2267-2278, 2015.

[27] R. Azimi, X. Zhan and S. Reda, "How Good Are Low-Power 64-bit SoCs for Server-Class Workloads?," in *IEEE International Symposium on Workload Characterization* (**IISWC**), pp. 116-117, 2015.

[28] S. Hashemi, R. I. Bahar and S. Reda, "DRUM: A Dynamic Range Unbiased Multiplier for Approximate Applications," in ACM/IEEE International Conference on Computer-Aided Design, pp. 418-425, 2015. (**ICCAD**) **Best Paper Candidate (4 selected out of 382 submissions)**. Acceptance rate 24.6%.

[29] S. Jayakumar, S. Reda, "Making Sense of Thermoelectrics for Processor Thermal Management and Energy Harvesting," in *IEEE/ACM International Symposium on Low-Power Electronics and Design* (**ISLPED**), pp. 31-36, 2015. Full paper acceptance rate 19.6%.

[30] **J** A. N. Nowroz, K. Hu, F. Koushanfar, S. Reda, "Novel Techniques for High-Sensitivity Hardware Trojan Detection using Thermal and Power Maps", in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 33(12), pp.1792-1805, 2014.

[31] **J** red Ulusel, K. Nepal, R. I. Bahar and S. Reda, "Fast Design Exploration for Performance, Power and Accuracy Tradeoffs in FPGA-based Accelerators, in ACM Transactions on Reconfigurable Technology and Systems, Vol 7(1), pp. 4:1–4:22, 2014.

[32] R. Azimi, X. Zhan and S. Reda, "Thermal-aware Layout Planning for Heterogeneous Datacenters", in IEEE/ACM International Symposium on Low-Power Electronics and Design (**ISLPED**), pp. 245-250, 2014.

[33] K. Nepal, Y. Li, R. I. Bahar and S. Reda, "ABACUS: A Technique for Automated Behavioral Synthesis of Approximate Computing Circuits," in *IEEE/ACM Design, Automation and Test in Europe* (**DATE**), 2014. Acceptance rate 23.1%

[34] **J** A. Nowroz, G. Woods and S. Reda, "Power Mapping of Integrated Circuits Using AC-based Thermography," in *IEEE Transactions on Very Large Scale Integration*, Vol. 21(8), pp. 1398-1409, 2013.

[35] **J** S. Reda, A. N. Nowroz, and R. Cochran, "Post-Silicon Power Mapping Techniques for Integrated Circuits," in *ElSevier VLSI Integration*, Vol 46, pp. 69-79, 2013.

[36] K. Dev, A. N. Nowroz and S. Reda, "Power Mapping and Modeling of Multi-core Processors," in *IEEE International Symposium on Low-Power Electronics and Design* (**ISLPED**), pp. 39-44, 2013. Acceptance rate 35%.

[37] C. Hankendi, S. Reda and A. Coskun, "vCap: Adaptive Power Capping for Virtualized Servers," in *IEEE International Symposium on Low-Power Electronics and Design* (**ISLPED**), pp. 415-420, 2013. Acceptance rate 35%.

[38] X. Zhan and S. Reda, "Techniques for Energy-Efficient Power Budgeting in Data Centers," in *IEEE/ACM Design Automation Conference* (**DAC**), Article No. 176, 2013. Acceptance rate 21.7%.

[39] K. Dev, G. Woods and S. Reda, "High-Throughput TSV Testing and Characterization for 3D Integration Using Thermal Mapping," in *IEEE/ACM Design Automation Conference* (**DAC**), Article No. 73, 2013. Acceptance rate 21.7%.

[40] F. Paterna and S. Reda, "Mitigating Dark Silicon Problems Using Superlattice-based Thermoelectric Coolers," *Design, Automation and Test in Europe* (**DATE**), pp. 1391-1394, 2013. Acceptance rate 30%.

[41] K. Hu, A. Nowroz, S. Reda and F. Koushanfar, "High-Sensitivity Hardware Trojan Detection Using Multimodal Characterization Power Mapping of Integrated Circuits Using AC-based Thermography," in *Design, Automation and Test in Europe* (**DATE**), pp. 1271-1276, 2013. Acceptance rate 30%.

[42] **J** R. Cochran and S. Reda, "Thermal Prediction and Adaptive Control Through Workload Phase Detection," in ACM Transactions on Design Automation of Electronic Systems, Vol 18(1), 7:1-7:19, 2012.

[43] K. Nepal, red Ulusul, R. I. Bahar and S. Reda, "Fast Multi-Objective Algorithmic-Design Co-Exploration for FPGA-based Accelerators," *IEEE International Symposium on Field-Programmable Custom Computing Machines (***FCCM***)*, pp. 65-68, 2012.

[44] **J** S. Reda, R. Cochran and A. Coskun, "Adaptive Power Capping for Servers with Multi-Threaded Workloads," in IEEE MICRO, Vol 32(5), pp. 64-75, 2012.

[45] **J** S. Reda and A. N. Nowroz, "Power Modeling and Characterization of Computing Devices: A Survey," in Foundations and Trends in Electronic Design Automation, NOW Publishers, Vol. 6(2), pp. 121 – 216, 2012. Also available in a book format.

[46] **J** S. Reda, "Thermal and Power Characterization Techniques for Real Computing Systems," *IEEE Journal on Emerging Topics in Circuits and Systems,* Vol 1(2), pp. 76 – 87, 2011.

[47] **J** S. Reda, R. Cochran and A. N. Nowroz, "Improved Thermal Tracking for Processors Using Hard and Soft Sensor Allocation Techniques," *IEEE Transactions on Computers,* Vol. 60(6), pp. 841-861, 2011.

[48] R. Cochran, C. Hankendi, A. Coskun and S. Reda, "Pack & Cap: Adaptive DVFS and Thread Packing Under Power Caps," *IEEE/ACM International Symposium on Microarchitecture (***MICRO***)*, pp. 175-185, 2011. Acceptance rate 21%.

[49] R. Cochran, C. Hankendi, A. Coskun and S. Reda, "Identifying the Optimal Energy-Efficient Operating Points of Parallel Workloads," *ACM/IEEE International Conference on Computer-Aided Design (***ICCAD***)*, pp. 608-615, 2011. Acceptance rate 30%.

[50] A. N. Nowroz and S. Reda, "Improved Post-Silicon power Modeling Using AC Lock-In Techniques," in proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, pp. 101-106, 2011. Acceptance rate 23%.

[51] A. N. Nowroz and S. Reda, "Thermal and Power Characterization of Field-Programmable Gate Arrays," in proceedings of *ACM International Symposium on Field Programmable Gate Arrays (***FPGA***)*, pp. 111-114, 2011. Full + short paper acceptance rate 43%.

[52] **J** S. Reda and S. Nassif, "Accurate Spatial Estimation and Decomposition Techniques for Variability Characterization," *IEEE Transactions on Semiconductor Manufacturing,* 23(3), 2010, pp. 345-357.

[53] N. H. Khan, S. Reda and S. Hassoun, "Early Estimation of TSV Area for Power Delivery in 3D Integrated Circuits," in proceedings of *IEEE International 3D Systems Integration Conference (***3D-IC***)*, pp. 1–6, 2010.

[54] R. Cochran, A. Nowroz and S. Reda , "Post-Silicon Power Characterization Using Thermal Infrared Emissions," in proceedings of *ACM/IEEE International Symposium on Low-Power Electronics and Design (***ISLPED***)*, pp. 331-336, 2010. **Best Paper Award (2 out of 203 papers)**. Full paper acceptance rate 23%.

[55] J. Qiu, S. Reda and S. Hassoun, "Fast, Accurate Routing Delay Estimation," in proceedings of *ACM System Level Interconnect Prediction Workshop (***SLIP***)*, pp. 77–82, 2010.

[56] A. Nowroz, R. Cochran and S. Reda, "Thermal Monitoring of Real Processors: Techniques for Sensor Allocation and Full Characterization," proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, pp. 56–61, 2010. Acceptance rate 24%.

[57] R. Cochran and S. Reda, "Consistent Runtime Thermal Prediction and Control Through Workload Phase Detection," in proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, pp. 62–67, 2010. Acceptance rate 24%.

[58] **J** S. Reda, G. Smith and L. Smith, "Maximizing the Functional Yield of Wafer-to-Wafer 3D Integration," *in IEEE Transactions on Very Large Scale Integration Systems,* 17(9), 2009, pp. 1357-1362.

[59] S. Reda, R. I. Bahar and A. Si, "Reducing the Leakage and Timing Variability of 2D ICs Using 3D ICs," in proceedings of *ACM/IEEE International Symposium on Low Power Electronics and Design (***ISLPED***)*, pp. 283–286, 2009. Acceptance rate 35%.

[60] R. Cochran and S. Reda, "Spectral Techniques for High-Resolution Thermal Characterization with Limited Sensor Data," in proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, pp. 478–483, 2009. Acceptance rate 22%.

[61] S. Reda, "Using Circuit Structural Analysis Techniques for Networks in Systems Biology," in proceedings of *ACM System Level Interconnect Prediction (***SLIP***)*, pp. 37–44, 2009. Acceptance rate 52%.

[62] R. Le, S. Reda and R. I. Bahar, "High-Performance, Cost-Effective Heterogeneous 3D FPGA Architectures," in proceedings of *ACM Great Lakes VLSI Symposium (***GLSVLSI***)*, pp. 251–256, 2009. Acceptance rate 46%.

[63] M. Kadin, S. Reda and G. Uht, "Central vs. Distributed Dynamic Thermal Management for Multi-Core Processors: Which One is Better?," in proceedings of *ACM Great Lakes VLSI Symposium (***GLSVLSI***)*, pp. 137–140, 2009. Acceptance rate 46%.

[64] S. Reda and S. Nassif, "Analyzing the Impact of Process Variations on Parametric Measurements: Novel Models and Applications," in proceedings of *IEEE Design, Automation, Test in Europe (***DATE***)*, 2009, pp. 375–380. Accepting rate 23%.

[65] **J** C. Ferri, S. Reda and R. I. Bahar, "Parameteric Yield Management of 3D ICs: Models and Strategies for Improvement," *ACM Journal on Emerging Technologies in Computing Systems. Special issue on 3D ICs.* 4(4), 2008, pp. 19:1 – 19:22.

[66] M. Kadin and S. Reda, "Frequency and Voltage Planning for Multi-Core Processors Under Thermal Constraints," in proceedings of *IEEE International Conference on Computer Design (***ICCD***)*, pp. 463 – 470, 2008. Acceptance rate 34%.

[67] M. Kadin and S. Reda, "Frequency Planning for Multi-Core Processors Under Thermal Constraints," in proceedings of *IEEE/ACM International Symposium on Low Power Electronics and Design (***ISLPED***)*, pp. 213 – 216, 2008. Acceptance rate 40%.

[68] B. Hargreaves, H. Hult and S. Reda, "Within-die Process Variations: How Accurately Can They Be Statistically Modeled?," in proceedings of *IEEE Asian South Pacific Design Automation Conference (***ASPDAC***)*, pp. 524 – 530, 2008. **Best Paper Candidate (10 out of 350 submitted papers)**. Acceptance rate 28%.

[69] D. Meisner and S. Reda, "Hardware Libraries: An Architecture for Economic Acceleration in Soft Multi-Core Environments," in proceedings of *IEEE International Conference on Computer Design (***ICCD***)*, 2007, pp. 189 – 196. Acceptance rate 27%.

[70] C. Ferri, S. Reda and R. I. Bahar, "Strategies for Improving the Parametric Yield and Profits of 3D ICs," in proceedings of *ACM/IEEE International Conference on Computer-Aided Design (***ICCAD***)*, 2007, pp. 220 – 226. Acceptance rate 33%.

[71] A. B. Kahng, S. Reda and P. Sharma, "On-Line Adjustable Buffering for Runtime Power Reduction," in proceedings of *IEEE International Symposium on Quality Electronic Design Automation (***ISQED***)*, 2007, pp. 550 – 555. Acceptance rate 31%.

[72] **J** A. B. Kahng and S. Reda, "Zero-Change Netlist Transformations: A New Technique for Placement Benchmarking," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(12), 2006, pp. 2806 – 2819.

[73] **J** A. B. Kahng and S. Reda, "Wirelength Minimization for Min-Cut Placements via Placement Feedback," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(7), 2006, pp. 1301 – 1312.

[74] **J** C. Alpert, A. B. Kahng, G-J. Nam, S. Reda and P. Villarubia, "A Fast Hierarchical Quadratic Placement Algorithm," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(4), 2006, pp. 678 – 691.

[75] **J** A. B. Kahng and S. Reda, "New and Improved BIST Diagnosis Techniques from Combinatorial Group Theory," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(3), 2006, pp. 533 – 543.

[76] **J** A. B. Kahng, I. Măndoiu, S. Reda, A. Zelikovsky and X. Xu, "Computer-Aided Optimization of DNA Array Design and Manufacturing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25(2), 2006, pp. 305 – 320.

[77] A. B. Kahng and S. Reda, "A Tale of Two Nets: Studies in Wirelength Progression in Physical Design," in proceedings of *ACM System-Level Interconnect Prediction (***SLIP***),* 2006, pp. 17 – 24.

[78] S. Reda and A. Chowdhary, "Effective Linear Programming Based Placement Methods," in proceedings of *ACM International Symposium on Physical Design (***ISPD***),* 2006, pp. 186 – 191. Acceptance rate 35%.

[79] **J** A. B. Kahng and S. Reda, "Intrinsic Shortest Path Length: A New, Accurate A Priori Wirelength Estimator," in proceedings of *ACM/IEEE International Conference on Computer-Aided Design (***ICCAD***),* 2005, pp. 173 – 180. Acceptance Rate 25%.

[80] A. B. Kahng, S. Reda and Q. Wang, "Architecture and Details of a High Quality, Large-Scale Analytical Placer," in proceedings of *ACM/IEEE International Conference on Computer-Aided Design (***ICCAD***)*, 2005, pp. 891 – 898. **Best Paper Candidate.** Acceptance Rate 25%.

[81] Y. Cheon, P-H. Ho, A. Kahng, S. Reda and Q. Wang, "Power-Aware Placement," in proceedings of *ACM/IEEE Design Automation Conference (***DAC***)*, 2005, pp. 795 – 800. Acceptance rate 24%.

[82] A. B. Kahng and S. Reda, "Evaluation of Placer Suboptimality via Zero-Change Transformations," in proceedings of *ACM International Symposium on Physical Design (***ISPD***)*, 2005, pp. 208 – 215. Acceptance rate 37%.

[83] C. Alpert, A. B. Kahng, G-J. Nam, S. Reda and P. Villarubia, "A Semi-Persistent Clustering Technique for VLSI Circuit Placement," in proceedings of *ACM International Symposium on Physical Design (***ISPD***)*, 2005, pp. 200 – 207. Acceptance rate 37%.

[84] A. B. Kahng, S. Reda and Q. Wang, "APlace: A General Analytic Placement Framework," in proceedings of *ACM International Symposium on Physical Design (***ISPD***)*, 2005, pp. 233 – 235. **Winner of the ISPD-2005 VLSI Placement Contest.**

[85] **J** A. B. Kahng and S. Reda, "Match Twice and Stitch: A New TSP Tour Construction Heuristic," *Operations Research Letters*, 2004, 32(6), pp. 449 – 509. **"Hot" (most downloaded) article in Operations Research Letters, February 2005.**

[86] **J** A. B. Kahng, I. Măndoiu, P. Pevzner, S. Reda and A. Zelikovsky, "Scalable Heuristics for Design of DNA Probe Arrays," *Journal of Computational Biology*, Vol. 11(2-3), 2004, pp. 429 – 447.

[87] A. B. Kahng and S. Reda, "Reticle Floorplanning With Guaranteed Yield for Multi-Projects Wafer," in proceedings of *IEEE International Conference on Computer Design (***ICCD***)*, 2004, pp. 106 – 110. Acceptance rate 37%.

[88] A. B. Kahng and S. Reda, "Placement Feedback: A Concept and Method for Better Min-Cut Placements," in proceedings of *ACM/IEEE. Design Automation Conference (***DAC***)*, 2004, pp. 357 – 362. Acceptance rate 25%.

[89] A. B. Kahng, I. Markov and S. Reda, "On Legalization of Row-Based Placements," in proceedings of *ACM Great Lakes VLSI Symposium (***GLSVLSI***)*, 2004, pp. 214 – 219. Acceptance rate 40%.

[90] A. B. Kahng, I. Markov and S. Reda, "Boosting: A Min-Cut Placement with Improved Signal Delay," in proceedings of *IEEE Design Automation and Test in Europe (***DATE***)*, 2004, pp. 1098 –1103. Acceptance rate 27%.

[91] A. B. Kahng and S. Reda, "Combinatorial Group Testing Methods for the BIST Diagnosis Problem," in proceedings of *IEEE Asia South Pacific Design Automation Conference (***ASPDAC***)*, 2004, pp. 113 – 116. Acceptance rate 50%.

[92] A. B. Kahng, I. Măndoiu, S. Reda, X. Xu and A. Zelikovsky, "Evaluation of Placement Techniques for DNA Probe Array Layout," in proceedings of *ACM/IEEE International Conference in Computer-Aided Design (***ICCAD***)*, 2003, pp. 262 – 269. Acceptance Rate 26%.

[93] A. B. Kahng, I. Măndoiu, S. Reda, A. Zelikovsky and X. Xu, "Design Flow Enhancements for DNA Arrays," in proceedings of *IEEE International Conference on Computer Design (***ICCD***)*, 2003, pp. 116 – 123. Acceptance rate 33.4%.

[94] A. B. Kahng, I. Măndoiu, P. Pevzner, S. Reda and A. Zelikovsky, "Engineering a Scalable Placement Heuristic for DNA Probe Arrays," in proceedings of *ACM International Conference on Research in Computational Molecular Biology (***RECOMB***)*, 2003, pp. 148 – 156. Acceptance rate 20%.

[95] A. B. Kahng, I. Măndoiu, P. Pevzner, S. Reda and A. Zelikovsky, "Border Length Minimization in DNA Array Design," in proceedings of Springer-Verlag Lecture Notes in Computer Science Series 2452, *Workshop on Algorithms in Bioinformatics (***WABI***)*, 2002, pp. 435–448.

[96] S. Reda and A. Orailoğlu, "Reducing Test Application Time through Test Data Mutation," in proceedings of *IEEE Design Automation and Test in Europe (***DATE***)*, 2002, pp. 387 – 393. **Best Paper Award (3 out of 476 papers)**. Acceptance rate 18% for full papers.

[97] S. Reda, R. Drechsler and A. Orailoğlu, "On the Relation between BDDs and SAT for Equivalence Checking," in proceedings of *IEEE International Symposium on Quality Electronic Design Automation (***ISQED***)*, 2002, pp. 394 – 399.

[98] S. Reda and A. Salem, "Combinational Equivalence Checking using Boolean Satisfiability and Binary Decision Diagrams," in proceedings of *IEEE Design Automation and Test in Europe (***DATE***)*, 2001, pp. 122 – 126. Acceptance rate 27% for full papers.

[99] S. Reda, A. Wahba, A. Salem, D. Borrione and A. Ghonaimy, "On the Use of Don't Cares during Reachability Analysis," in proceedings of *IEEE International Symposium on Circuits and Systems (***ISCAS***)*, 2001, pp. 121 – 124.

Patents

[1] S. Reda, A. Nowroz and K. Dev, "Power Mapping and Modeling System for Integrated Circuits", *US Patent*, US20160124443A1.

[2] C. Alpert, G-J. Nam, S. Reda and P. Villarubia, "Clustering Techniques for Faster and Better Placement of VLSI Circuits," *US Patent*, US7296252.

Workshop Papers, Posters and Technical Reports

[1] H. Tann, S. Hashemi and S. Reda, "Flexible Deep Neural Network Processing," arXiv Technical Report 1801.07353, 2018.

[2] S. Steffl and S. Reda, "LACore: A RISC-V Based Linear Algebra Accelerator for SoC Designs", RISCV workshop, 2017.

[3] M. Shalan and S. Reda "Cloud-Based RISC-V SoC design and Co-simulation", RISCV workshop, 2017.

[4] H. Tann, S. Hashemi, R. I. Bahar and S. Reda "Hardware-Software Codesign Techniques for Deep Neural Networks" in BARC workshop 2017.

[5] S. Reda "Taking Control of On-chip Process and Thermal Variations: From Sensors and Models to Runtime Management Techniques", Design Technology Coupling workshop, 2016.

[6] S. Reda, "Energy-Efficient Nano-Scale Computing Using Approximate Circuits", National Academies of Science USA-Arab Symposium, 2016.

[7] S. Reda "New Frontiers for Infrared Sensing in Electrical and Computer Engineering", National Academies of Science USA-Arab Symposium, 2015.

[8] K. Nepal, Y. Li, R. I. Bahar and S. Reda, "Automated High-Level Synthesis of Low Power/Area Approximate Computing Circuits", Workshop on Approximate Computing Across the Stacks (WACAS), 2014.

[9] S. Reda, "Using Infrared Imaging to Improve Integrated Circuit Design", CANDE workshop 2011.

7. GRANTS

Total (PI or co-PI): $20.08M. Brown Total (PI or co-PI): $8.55M.

1. Title: **Novel SW/HW Approximate Computing Methodologies with Case Studies on Biometric Security Systems**
   Agency & Program: NSF SHF
   Total Amount / Brown Share: $331K
   Start Date: July 2018
   Role: sole PI
2. Title: **A SW/HW Sensory-Rich Monitoring System for SoC Designs**
   Agency & Program: DARPA POSH Program
   Total Amount / Brown Share: $611K
   Start Date: June 2018
   Role: PI (co-PI: J. Rosenstein)
3. Title: **OpenROAD: Foundations and Realization of Open, Accessible Design**
   Agency & Program: DARPA IDEA Program
   Total Amount / Brown Share: $11.38M / $0.8M
   Start Date: June 2018
   Role: co-PI (PI: A. B. Khang at UCSD)
4. Title: **Research in Energy Efficiency of Augmented Reality Headsets**
   Agency & Program: Oculus Research
   Total Amount / Brown Share: $25K
   Start Date: 02/2018
   Role: Sole PI
5. Title: **Chemical CPUs: Chemical Computational Processing via Ugi Reactions**
   Agency & Program: DARPA Molecular Informatics Program
   Total Amount / Brown Share: $4.15M
   Start Date: 01/2018
   Role: co-PI (PI: B. Rubstein with J. Rosenstein, J. Rose, J. Sello, E. Kim and P. Weber)
6. Title: **An Integrated Framework for Thermal / Power Sensing and Management**
   Agency & Program Samsung GRO
   Total Amount / Brown Share: $100K
   Start Date: 11/2017
   Role: Sole PI
7. Title: **Modeling the Next-Generation Hybrid Cooling Systems for High-Performance Processors**
   Agency & Program: NSF CRI
   Total Amount / Brown Share: $696K / $231K
   Start date: 2017
   Role: PI (Lead PI: A. Coskun and E. Wang)
8. Title: **FPGA Implementation of Feature Extraction Algorithms for an Iris Recognition Scanner**
   Agency & Program: RI RICC with Videology
   Total Amount / Brown Share: $50K

Start date: 2017
Role: PI

9. Title: **Open Cloud-based Digital ASIC design Environment**
Agency & Program: Egypt Academy of Scientific Research and Technology JESOR program
Total Amount / Brown Share: EGP 980K / – (equivalent to $111K at the time)
Start date: 2016
Role: co-PI Consultant with PI M. Shalan

10. Title: **Blind Source Separation for Improved Power Characterization through Infrared Imaging**
Agency & Program: US National Academy of Science, Engineering & Medicine US-Arab Fellowship
Total Amount / Brown Share: $2.5K
Start date: 2016
Role: PI with A. Belouchrani

11. Title: **Symbiotic Power Management for Integrated CPU - GPU Platforms**
Agency & Program: NSF XPS
Total Amount / Brown Share: $316K with REU.
Start date: 2014
Role: Sole PI.

12. Title: **Automatic High-Level Synthesis of Approximate Computing Circuits**
Agency & Program: NSF SHF
Total Amount / Brown Share: $458K with REU
Start date: 2014
Role: PI (with co-PI R. I. Bahar)

13. Title: **Enabling Autonomous Flight of Drones in Complex, Unpredictable Environments**
Agency & Program: Brown Seed
Total Amount / Brown Share: $80K
Start date: 04/2014
Role: co-PI (with R. I. Bahar, J. Kellner and O. C. Jenkins)

14. Title: **Power Mapping and Modeling of a APU Using Thermal Infrared Emission Measurements**
Agency & Program: AMD Corporation
Total Amount / Brown Share: $25K
Start date: 07/2013
Role: Sole PI

15. Title: **II-NEW: A Platform to Advance Research in Energy-Efficient Computing**
Agency & Program: NSF CRI
Total Amount / Brown Share: $190K
Start date: 2013
Role: Sole PI

16. Title: **Processing of Large Wide Area Airborne Sensor Data Streams in Hardware**
Agency & Program: DoD ONR SBIR with Videology
Total Amount / Brown Share: $26K
Start date: 2012
Role: co-PI (with R. I. Bahar)

17. Title: **Power Mapping of Many-Core Processors**
    Agency & Program: Intel Corporation
    Amount: $85K
    Start date: 07/2011
    Role: Sole PI

18. Title: **Algorithmic Techniques for Post-Silicon Characterization Using Infrared Emissions**
    Agency & Program: NSF SHF
    Total Amount / Brown Share: $400K / $200K
    Start date: 06/2011
    Role: Lead PI (w. F. Koushanfar and G. Woods)

19. Title: **CAREER: Transcending the Thermal Challenges of Tera-Scale Computing**
    Agency & Program: NSF CAREER
    Total Amount / Brown Share: $443 with REU
    Start date: 02/2010
    Role: Sole PI

20. Title: **Wide Area Video Motion Blur Elimination**
    Agency & Program: DARPA SBIR with ObjectVideo Inc
    Total Amount / Brown Share: $180K
    Start date: 03/2010
    Role: co-PI (with R. I. Bahar and J. Mundy)

21. Title: **Adaptive Hot Spot Cooling for Many-Core Processors**
    Agency & Program: DAC Newton Award
    Total Amount / Brown Share: $24K.
    Start date: 06/2010
    Role: Sole PI

22. Title: **An Infrared System for Thermal-Driven Research in Computer Vision and Electronics**
    Agency & Program: DoD DURIP (ARL)
    Total Amount / Brown Share: $180K
    Start date: 07/2009
    Role: PI (with R. I. Bahar and J. Mundy)

23. Title: **Yield Optimization Techniques for 3D Integrated Circuits**
    Agency & Program: Qualcomm Corporation
    Total Amount / Brown Share: $25K
    Start date: 05/2008
    Role: Sole PI

24. Title: **ProHunter: A Platform to Accelerate Protein Identification from Mass-Spectrometry Data**
    Agency & Program: Brown Salomon award
    Total Amount / Brown Share: $15K
    Start date: 12/2007
    Role: Sole-PI

25. **Equipment Donations:**

    - Altera, equivalent of $24K, 2006

- Nvidia, equivalent of $3.2K, 2015

26. **UTRA grants (each at $3.5K):**
    - J. Sriram 2010
    - R. Sailor 2011
    - M. Baxter 2012
    - J. Y. Wu 2014
    - W. Gonzalez 2016
    - M. Lee 2017
    - J. Vexler 2017

8. INVITED TALKS AND TUTORIALS

1. Samsung SARC Symposium, "Runtime Techniques for Thermal/Power Modeling and Management", Austin, TX, 10/17/2017.
2. Tufts University, "Energy-Efficient Approximate Computing", Medford, MA, 9/20/2017.
3. Samsung SARC, "Techniques for Thermal and Power Characterization and Modeling of Integrated Circuits", Austin, TX, 6/20/2017.
4. University of Rochester, "Energy-Efficient Approximate Computing", Rochester, NY, 3/16/2017.
5. WPI, "Energy-Efficient Approximate Computing: From Circuits to Systems", Worcester, MA, 1/1/2017.
6. NIST, "New Directions for Energy-Efficient Computing Systems: From Power Measurement to Control", Colarado, Boulder, 1/17/2017.
7. ICCAD Panel on Challenges and Opportunities of Stochastic Computing in the Dusk of Moores Law and the Dawn of Big Data, "Approximate Accelerator Design", ICCAD, Nov 8, 2016.
8. Masdar Institute, "Energy-Efficient Nano-Scale Computing Using Approximate Circuits", National Academy of Sciences Arab-American Frontiers Symposium, 11/6/16.
9. ETSI Media Workshop, "Scheduling Challenges and Opportunities in Integrated CPU+GPU Processors", Oct 7, 2016.
10. Google Hardware Platform Engineering, "New Techniques for Power Capping and Management for Datacenters", Sept 12 2016.
11. System Design for Cloud Services Workshop, "Optimal Decentralized Power Management for Large-Scale Computing Clusters", Microsoft Faculty Summit, July 15 2016.
12. Keynote Speaker, Design Technology Workshop, "Taking Control of On-chip Process and Thermal Variations: From Sensors and Models to Runtime Management Techniques", University of Munich. 6/29/16.
13. Infineon Semiconductors, "Reducing the Cost of Variability Sensing," Munich. 6/29/16.
14. ARL, "New Directions for Energy-Efficient Computing", Army Research Lab, Aberdeen, MD. 3/1/16.
15. KAUST, "New Frontiers for Infrared Sensing for Electrical and Computer Engineering", National Academy of Sciences Arab-American Frontiers Symposium, 12/5/15.
16. Microsoft Research, "Dealing with the Performance and Power Challenges of Data Centers," 3/21/14.
17. AMD Research, "How Hot is Your Hot Chip? And How to Deal with It?," 7/22/13.
18. DAC tutorial, "Avoiding Core Meltdown! - Adaptive Techniques for Power and Thermal Management of Multi-Core Processors," 6/3/13.
19. University of California, Los Angeles, "Re-thinking Power Characterization and Management Techniques for Computing Systems," 7/27/12.

20. CMOS Emerging Technologies Conference "Addressing the Thermal Challenges in Emerging Computing Platforms", 7/18/12.

21. Tutorial in International Green Computing Conference, "Thermal Imaging and Sensing", 6/8/12.

22. University of Virginia, "Re-thinking Power Characterization and Management Techniques for Computing Systems", 4/27/12.

23. University of Illinois, Chicago, "Re-thinking Power Characterization and Management Techniques for Computing Systems", 4/20/12.

24. University of California, Berkeley, "Rethinking Power Characterization Techniques of Integrated Circuits", 2/10/12.

25. University of Minnesota, Twin Cities, "From milliWatts to megaWatts: Re-thinking Power Characterization and Management Techniques for Computing Systems", 12/13/11.

26. The CANDE (Computer-Aided Network DEsign) workshop, San Jose, "Using Infrared Imaging to Improve Integrated Circuit Design," 11/10/11.

27. Qualcomm corporation, San Diego, "Rethinking Power Characterization Techniques of Computing Devices," 6/1/11.

28. University of California, San Diego, CSE seminar "Rethinking Power Characterization Techniques of Computing Devices," 6/1/11.

29. Intel Corporation, Portland, "Rethinking Power Characterization Techniques of Computing Devices," 2/16/11.

30. Boston University, ECE seminar, "Addressing the Thermal and Power Challenges of Tera-Scale Computing," 12/8/10.

31. Columbia University, CISL EE seminar, "Addressing the Thermal and Power Challenges of Tera-Scale Computing," 12/3/10.

32. IBM T. J. Watson Research Center, Yorktown, "New Approaches for Thermal and Power Characterization," 10/27/10.

33. Harvard University EE seminar series, "Addressing the Thermal and Power Challenges of Tera-Scale Computing," 10/22/10.

34. Qualcomm Corporation, San Diego, "Thermal Characterization and Post-Silicon Power Validation: Techniques and Experimental Setup," 7/6/10.

35. Waseda University, Tokyo, "Thermal Management Solutions for Tera-Scale Computing," 9/7/09.

36. Qualcomm Corporation, San Diego, "Models for Variability Characterization and Yield Improvement for Planar and 3D ICs," 8/20/09.

37. National Tsing Hua University, Hsinchu City, Taiwan, "Yield Improvement Techniques for 3D IC Technology," 9/9/08.

38. Freescale Semiconductor Corporation, Austin TX, "Yield Improvement Techniques for 3D IC Technology," 8/26/08.

39. IBM Austin Research Lab, Austin, TX, "How Accurate Can Process Variations be Statistically Modeled and Analyzed?," 8/25/08.

40. Intel Corporation, Bangalore, "3D IC Technology: Opportunities and Challenges," 8/13/08.

41. University of California, Los Angeles, "Accurate Extraction and Statistical Modeling of Within-die Process Variations," 6/4/08.

42. University of Rhode Island, "Maximizing the Physical Performance of Multi-Core Processors Under Thermal Constraints," 6/2/08.

43. Seoul National University, "Economic Acceleration in SoC Designs Using Hardware Libraries," 9/8/07.

44. Qualcomm Corporation, San Diego, "Addressing the Challenges of Process Variations Modeling and Yield Improvement in 3D Integrated Circuits," 8/2/07.

45. Tufts University, Massachusetts, "VLSI Interconnects: Realistic Benchmarking of Optimizations and Accurate Estimation of Characteristics," 10/5/06.

46. Iowa State University, “From VLSI Circuits to Gene Chips: New Approaches to Placement and Benchmarking,” 4/17/06.
47. Boston University, “From VLSI Circuits to Gene Chips: New Approaches to Placement and Benchmarking,” 3/22/06.
48. Brown University, “From VLSI Circuits to Gene Chips: New Approaches to Placement and Benchmarking,” 3/21/06.
49. UC, Riverside, “From VLSI Circuits to Gene Chips: New Approaches to Placement Benchmarking,” 3/10/06.
50. UC, Santa Cruz, “From VLSI Circuits to Gene Chips: New Approaches to Placement Benchmarking,” 2/15/06.

9. OPEN-SOURCE RESEARCH SOFTWARE/ARTIFACT RELEASES

All releases are available at `http://scale.engin.brown.edu/tools/` and `http://github.com/scale-lab`.

- **CloudV:** A cloud service (`http://cloudv.io`) for IC design based on open-source EDA tools.
- **LACore:** LACore is a linear algebra accelerator for RISC-V ecosystem.
- **ClusterSoCBench:** A parallel benchmark set to evaluate clusters made of SoC ARM processors.
- **BPI:** A blind power identification software for processors.
- **DPC:** A software tool for decentralized power capping of computing clusters.
- **ABACUS:** ABACUS is a high-level synthesis tool for approximate computing circuits.
- **DRUM:** HDL for an approximate multiplier with a dynamic range and unbiased error distribution.
- **Infrared imaging data:** Large collection of infrared imaging characterization data from FPGAs, dual core and quad-core processors.
- **MTS:** Software for calculating solution of the Traveling Salesman Problem based on our constructive TSP Match & Stitch technique.

10. MENTORING AND ADVISING

Current Research Group Members:

1. Dr. Mostafa Said (Oct 2017 –).
2. Dr. Soheil Hashemi (June 2018 –)
3. Dr. Chao Jing (Oct 2017 –)
4. Hokchhay Tann (PhD program, Fall 2014 –).
5. Sofiane Chetoui (PhD program, Fall 2017 –).
6. Heng Zhao (ScM program, Spring 2018),

Supervised PhD Theses:

1. Ryan J. Cochran, Ph.D. (2008 – 2012). First job position at Qualcomm.
   Thesis Title: “Techniques for Adaptive Power and Thermal Sensing and Management of Multi-core Processors”.
2. Nowroz Abdullah, Ph.D. (2009 – 2013). First job position at Intel.
   Thesis Title: “Power Mapping of Computing Devices: Fundamentals and Applications”.
3. Kumud Nepal, Ph.D. (2010 – 2015). Co-advised with R. I. Bahar. First job position at Oracle.
   Thesis Title: “New Directions for Design-Space Exploration of Low-Power Hardware Accelerators”.
4. Kapil Dev, Ph.D. (2011 – 2016). First job position at Nvidia.
   Thesis Title: “New Techniques for Power-Efficient CPU-GPU Processors”

5. Xin Zhan, Ph.D. (2012 – 2017). First job at Apple
   Thesis Title "Energy-Efficiency Optimization Techniques for Computing Clusters: Exploiting the Heterogeneities".

6. Soheil Hashemi, Ph.D (2013 – 2018).
   Thesis title "Approximate Computing Techniques for Accuracy Energy Trade-offs".

7. Reza Azimi, Ph.D. (2013 – 2018).
   Thesis title "Improving the Performance of Power Constrained Computing Clusters".

Supervised ScM Students:

1. Shuchen Zheng, Sc.M. (2015 – 2016). First job position at Facebook.
   Thesis Title: "Maximizing the performance of Parallel Applications on Heterogeneous CPU-FPGA System". First position at Facebook.

2. Kuiyuan Mao (Spring 2014) – course track.

3. Yueting Li (Spring 2013) – course track.

4. Roto Le (Fall 2008, Spring 2009) – course track.

5. Chakanetsa Zaraniyka (Fall 2008) – course track.

6. Brendan Hargreaves (Spring 2008) – course track.

Supervised Postdocs / visiting PhDs:

- Francesco Paterna (7/2012–12/2012).
- Morteza Nabavi Nejad (12/2016–5/2017)
- Chao Jing (10/2017 –)
- Mostafa Said (10/2017 –)

Supervised Undergraduate Honors Theses:

- Thesis advisor for Samuel Steffl 2017.
  Thesis title: "LACore: A Large-Format Vector Accelerator for Linear Algebra Applications".
- Thesis advisor for Tyler Fox 2017.
  Thesis title: "Revisiting The Case of ARM SoCs for High-Performance Computing Clusters".
- Thesis advisor for Sriram Jayakumar 2013.
  Thesis title: "Dynamic Thermal Management for Processors Using Thermoelectric Coolers".
- Thesis advisor for Natalie Serrino 2012.
  Thesis title: "Soft Power Capping for Improved Performance of Computing Systems".
- Thesis advisor for Shi-Qing Poh 2010.
  Thesis title: "Thermal Measurements and Characterizations for Real Processors".
- Thesis advisor for Michael Kadin 2008.
  Thesis title: "Performance Driven Frequency/Voltage Planning for Multi-Core Processors with Thermal Constraints".
- Thesis advisor for Aaron Mandle 2008.
  Thesis title: "FPGA Based Hardware Acceleration: A Case Study in Protein Identification".
- Thesis advisor for David Meisner 2007.
  Thesis title: "Design of a Shared Hardware Library for Multi-Core Environments in FPGA Fabrics".

Undergraduate Research Advising:

- Samuel Oliphant (Summer 2017)
- Myungjin Lee (Summer 2017)

- Jonathan Vexler (Summer 2017)
- Samuel Steffl (Fall 2016 and Spring 2017)
- Tyler Fox (Summer 2016, Fall 2016 and Spring 2017)
- Nicholas Anthony (Summer 2016)
- Wendy Gonzalez (Summer and Fall 2016, Spring 2018)
- Lucas Salla Pagnan (Spring 2016)
- Abdul Tabish (Spring 2016).
- Adam Cooper (Summer 2015).
- Casey Meehan (Fall 2013).
- Jie Ying Wu (Summer - Fall 2013).
- Sriram Jayakumar (Summer 2010 / Brown UTRA, Spring 2012, Spring 2013).
- Margaret Baxter (Summer 2012 Brown UTRA – Undergraduate Teaching and Research Awards)
- Patipan Prasertsom (Spring 2012)
- Natalie Serrino (Summer 2011 – Spring 2012)
- Stefan Angelevski (Summer 2011 – Spring 2012)
- Ryan Sailor (Summer 2011 – Brown UTRA)
- Patrick Temple (Summer 2010 – Spring 2011 / NSF REU – Spring 2012).
- Shi-Qing Poh (Spring 2009 – Spring 2010).
- Aung Si (Summer 2008 – Summer 2009).
- Bryant Mairs (Spring 2008).
- Aaron Mandle (Spring 2008).
- Michael Kadin (Summer 2007 – Spring 2008).
- David Meisner (Spring 2007).

PhD thesis committee:

- C. Ferri (Brown University).
- Y. Shi (Brown University).
- J. Gaudette (Brown University).
- D. Papagiannopoulou (Brown University).
- O. Uluel (Brown University).
- F. Paterna (University of Bologna).
- H. Chen (Boston University).
- C. Hankendi (Boston University).
- F. Kaplan ((Boston University).
- M. Martins (Brown University).
- C. Heelan (Brown University).

Undergraduate Honors theses reader: G. Howard, K. Jang, and L. Renick.

PRIME program advising: A. Rossi, B. Agma and A. Rathi.

Freshmen and sophomore advising: advisor for numerous freshmen and sophomore students.

Outreach advising:

- Research advisor for Allison Paul from Lasalle High School Academy (summer 2012 – Spring 2013).
- Research advisor for Christopher Chedid from Dartmouth High School Academy (summer 2016).

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11. COURSES

2012–
Scale: 1.00 (best) – 5.00

- ENGN 1640 Design of Computing Systems `http://scale.engin.brown.edu/classes/EN164S17/`
  - Spring 2017. Enrollment: 16. Effectiveness of instructor: 1.00.
  - Spring 2016. Enrollment: 14. Effectiveness of instructor: 1.38.
  - Spring 2014. Enrollment: 18. Effectiveness of instructor: 1.20.
  - Spring 2012. Enrollment: 14. Effectiveness of instructor: 1.33.
- ENGN 2910A Advanced Computer Architecture `http://scale.engin.brown.edu/classes/EN2910AF15/`
  - Fall 2015. Enrollment: 6. Effectiveness of instructor: 1.33.
  - Fall 2013. Enrollment: 12. Effectiveness of instructor: 1.17.
- ENGN 2911X Reconfigurable Computing `http://scale.engin.brown.edu/classes/EN2911XF14/`
  - Fall 2014. Enrollment: 23. Effectiveness of instructor: 1.33.
  - Fall 2012. Enrollment: 17. Effectiveness of instructor: 1.31.
- ENGN 0031 Honors Introduction to Engineering
  - Fall 2017 (Section instructor – K. S. Kim is lecture instructor; C. Bull is BDW instructor).
    Enrollment: 41 (S01: 26, S02: 16). Eff. of instructor: S01: 1.38, S02: 1.58, Avg: 1.45.
  - Fall 2016 (Section instructor – C. Briant is lecture instructor; C. Bull is BDW instructor).
    Enrollment: 38 (S01: 19, S02: 19). Eff. of instructor: S01: 1.93, S02: 2.07, Avg: 2.00.

2006–2012:
scale: 5.00 (best) – 1.00.

– Teaching assistant for courses in computer architecture (UCSD), compiler design (Ain Shams University), introduction to programming languages (Ain Shams University), and computing circuit design (Ain Shams University).

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12. BROWN UNIVERSITY SERVICE

- Affirmative Action Representative (Fall '15 – Spring '18)
- Reviewer for Salomon grants (2015 round)
- Research Advisory Board (Fall'15 –)
- Director of Graduate Studies, School of Engineering (Fall '14)
- Faculty Mentor for Assistant Professors (S. Tellex in Computer Science)
- Electrical Sciences and Computer Engineer graduate representative (Fall '12 – Spring '14)
- Member of the committee on core Engineering education (Fall '13)

Semester	Class	Level	Enrollment	Plan	Lecture	HWs/Labs	Helpfulness	Average
Spring 2011*	EN164	undergraduate	37	4.56	4.60	4.36	4.88	4.60/5.00
Spring 2010*	EN52†	undergraduate	80	4.31	4.29	4.12	4.21	4.23/5.00
Spring 2009*	EN52†	undergraduate	89	4.10	4.14	3.89	4.06	4.05/5.00
Fall 2009*	EN2911X	graduate	6	4.16	4.33	4.33	4.83	4.41/5.00
Spring 2008*	EN160	undergraduate	8	4.40	4.40	4.40	4.80	4.50/5.00
Fall 2008*	EN2911C	graduate	7	3.50	3.33	3.00	3.83	3.41/5.00
Spring 2007*	EN160	undergraduate	8	4.43	4.43	4.00	5.00	4.46/5.00
Fall 2007*	EN2911X	graduate	11	4.63	4.27	4.72	4.45	4.52/5.00
Fall 2006*	EN291S40	graduate	5	4.60	4.60	4.60	5.00	4.45/5.00

Table 1: Sample of class evaluations. †class co-taught with H. Silverman. *

- Member of the University committee on Master Education (Fall '13)
- Honors program co-chair (Fall '12 – Spring '13)
- Undergraduate fellowship advisor (Fall'12 and Fall '13). Secured NIST fellowships for four undergraduate students.
- Member of Computer Engineering Hiring Committee, 2011 - 2012 and 2010 - 2011.
- Freshmen and sophomore concentration fair advisor 2011.
- Discussion leader in OSP BEARCORE event 2011.
- Preparation (with R.I. Bahar and D. Pacifici) of the graduate brochures of the ESCE group 2011.
- Coordinator of the Computer Engineering Advisory board 2010.
- Vice Chair of Brown University Computing Advisory board (CAB / ITAB) Fall 2008 and Spring 2009.
- Member of Brown University Computing Advisory board (CAB / ITAB) Spring 2008, Fall 2008, Spring 2009, and Fall 2009.
- Member of Brown University Information Technology Project Review Committee (ITPRC) Fall 2008 and Spring 2009.
- Seminar organizer for the School of Engineering, 2009 – 2011.
- Advisor for IEEE Chapter at Brown University, 2009 – 2011.
- Freshmen/sophomore year advisor for academic years 2008 – 2011.
- Co-organizer for the 2008 ABET accreditation of the computer engineering program.
- Mentor for students in the Program on Innovation Management and Entrepreneurship Engineering (PRIME) 2007, 2008.

13. SERVICE TO PROFESSION

- Chair:
  - Financial chair for IEEE Great Lakes VLSI Symposium 2016.
  - Local Arrangements Chair, IEEE International Symposium on Workload Characterization (IIWSC) 2016.
  - General Chair for IEEE System Level Interconnect Prediction (SLIP) Workshop 2010
  - Technical Program Chair for IEEE System Level Interconnect Prediction (SLIP) Workshop 2009
  - Publicity Chair for IEEE System Level Interconnect Prediction (SLIP) Workshop 2007 – 2008
- Technical Program Committee Member:

  - IEEE Symposium on Low Power Electronics and Design (ISLPED), 2017, 2018.
  - IEEE International Symposium on Computer Architecture (External PC), 2017.
  - IEEE International Symposium on Workload Characterization, 2016, 2018.
  - IEEE International Symposium on Physical Design (ISPD) 2014, 2015, 2016.
  - IEEE/ACM Design Automation Conference (DAC) 2011 – 2013 and 2017 –. DAC 2012, 2013 best paper selection committee
  - IEEE Design, Automation and Test in Europe (DATE) 2011, 2012. DATE '2018 best paper selection committee.
  - IEEE International Conference on Computer Design (ICCD) 2010 – 2016
  - IEEE International Conference on VLSI Design 2010 – 2011
  - IEEE International Conference on Very Large Scale Integration (VLSI) SoC 2011, 2012, 2014
  - IEEE Asian and South Pacific Design Automation Conference (ASP-DAC) 2008 – 2010
  - ACM/IEEE International Conference on Computer-Aided Design (ICCAD) 2008 – 2011 and 2017 –. Subcommittee chair 2010-2011, best paper selection committee, 2016-2017.
  - IEEE Great Lakes VLSI Symposium (GLSVLSI) 2007 – 2008
  - IEEE International Design and Test (IDT) Workshop 2009 – 2010
  - IEEE System Level Interconnect Prediction Workshop (SLIP) 2007 – 2010
  - IEEE International Symposium on Defect and Fault Tolerance (DFT) in VLSI and Nanotechnology Systems 2015, 2016.
- Session Chair:
  - Design Automation Conference (DAC) 2009
  - Great Lakes VLSI Symposium (GLSVLSI) 2009
  - Asian and South Pacific Design Automation Conference (ASP-DAC) 2008
  - International Conference on Computer-Aided Design (ICCAD) 2008
  - ElSevier, Integration, VLSI
- Proposal Reviews:
  - National Science Foundation: 2008, Nov 2009, June 2012, February 2013, February 2016, March 2018.
  - Ralph E. Powe Junior Faculty Award review for Texas A&M University, 2017.
  - University of Texas, San Antonio, 2016.
  - Brown University Salomon Proposals 2015.
  - Canada's NSERC
  - Autonomous Province of Bolzano, Italy 2012.
  - Davidson Institute for Talent Development 2010.
- ACM Outstanding PhD Dissertation Award committee, 2015
- Panelist in IEEE senior member review panel (Providence, RI 6/14/2014).
- Associate Editor
  - ElSevier, Integration, VLSI Journal
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
  - ASP Journal on Low Power Electronics
- Reviewer for Conferences and Journals:
  - Nature
  - IEEE Computer Architecture Letters.
  - IEEE Transactions on Cloud Computing

  - IEEE Transactions on Components, Packaging and Manufacturing Technology
  - IEEE Transactions on Electron Devices
  - IEEE Transactions on Signal Processing
  - IEEE Design & Test Magazine
  - IEEE Transactions on Nanobioscience
  - IEEE Transactions on Transactions on Information Forensics & Security
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits
  - IEEE Transactions on Computers
  - IEEE Transactions on Signal Processing
  - IEEE Design and Test of Computers
  - IEEE Journal on Emerging Topics in Circuits and Systems
  - IEEE Transactions on Very Large Scale Integration
  - IEEE Transactions on Circuits and Systems
  - IEEE Transactions on Parallel and Distributed Systems
  - IEEE Transactions on Semiconductor Manufacturing
  - IEEE Transactions on Multi-Scale Computing Systems
  - Communications of the ACM
  - ACM Transactions on Design Automation of Electronic Systems
  - ACM Transactions on Embedded Computing Systems
  - ACM Journal of Emerging Technologies in Computing
  - ACM Transactions on Architecture and Code Optimization
  - Japan's IEICE journal
  - IET Circuits, Devices & Systems
  - Elsevier Integration: The VLSI Journal
  - Kuwait Journal of Science and Engineering
  - Journal of Universal Computer Science
  - Springer Journal of Computational Electronics
  - International Conference on Computer-Aided Design
  - Design Automation Conference
  - International Symposium on Physical Design
  - International On-Line Test Workshop
  - International Conference on Computer Design
  - System Level Interconnect Prediction Workshop
  - Asian and South Pacific Design Automation Conference
  - International Symposium on Circuits and Systems
  - VLSI Test Symposium
  - International Symposium on Computer Architecture
- Contributor to ACM SIGDA Newsletter
- Member of IEEE CEDA Council
- Senior Member of the Institute of Electrical and Electronic Engineers (IEEE)
- Member of the Association for Computing Machinery (ACM)